MC-8
Controller
Service Manual

Harman Specialty Group 3 Oak Park, Bedford, MA, 01730-1413 USA
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Part No. 070-17536 | Rev 0

DOCUMENT CONVENTIONS

This document contains general safety and service instructions for the MC-8. It is important to read this manual before attempting service instructions. Pay particular attention to safety instructions.

The following symbols are used in this document:

	Appears on the component to indicate the presence of uninsulated, dangerous voltage inside the enclosure – voltage that may be sufficient to constitute a risk of shock.
	Appears on the component to indicate important operating and maintenance instructions in the accompanying literature.
WARNING	Calls attention to a procedure, practice, condition or the like that, if not correctly performed or adhered to, could result in injury or death.
CAUTION	Calls attention to a procedure, practice, condition or the like that, if not correctly performed or adhered to, could result in damage or destruction to part or all of the product.
Note:	Calls attention to information that is essential to highlight.

IMPORTANT SAFETY INSTRUCTIONS

1. Read and keep these instructions.
2. Heed all warnings.
3. Follow all operation instructions.
4. Do not use this apparatus near water.
5. Clean only with a dry cloth.
6. Do not block any ventilation openings.
7. Install in accordance with the manufacturer's instructions.
8. Do not install near any heat sources such as radiators, heat registers, stoves, or another apparatus (including amplifiers) that produces heat.
9. Do not defeat the safety purpose of the polarized or grounding-type plug. A polarized plug has two blades with one wider than the other. A grounding-type plug has two blades and a third grounding prong. The wide blade or the third prong are provided for your safety. If the provided plug does not fit into your outlet, consult an electrician for replacement of the obsolete outlet.
10. Protect the power cord from being walked on or pinched particularly at plugs, convenience receptacles, and the point where they exit from the apparatus.
11. Only use attachments/accessories specified by the manufacturer.
12. Use only with the cart, stand, tripod, bracket, or table specified by the manufacturer, or sold with the apparatus. When a cart is used, use caution when moving the cart/apparatus combination to avoid injury from tip-over.

13. Unplug this apparatus during lightning storms or when unused for long periods of time.
14. Refer all servicing to qualified service personnel. Servicing is required when the apparatus has been damaged in any way, such as when a power-supply cord or plug is damaged, liquid has been spilled or objects have fallen into the apparatus, the apparatus has been exposed to rain or moisture, does not operate normally, or has been dropped.
15. Refer to the operating instructions for power requirements. Be advised that different operating voltages may require the use of different line cord and/or attachment plug.
16. Do not install the unit in an unventilated rack, or directly above heat-producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.
17. Never attach audio power amplifier outputs directly to any of the unit's connectors.
18. To reduce the risk of fire or electric shock, do not expose this apparatus to rain or moisture.
19. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and radiates radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on. The user is encouraged to try to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ television technician for help.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this unit. Failure to comply with these precautions or with specific warnings elsewhere in these instructions violates manufacturer safety standards and intended use of this unit. Harman Specialty Group assumes no liability for failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard, the unit chassis and cabinet must be connected to an electrical ground. The unit is equipped with a three-wire grounding type plug. It will only fit into a grounding type power outlet. This is a safety feature. If you are unable to insert the plug into the outlet, contact your electrician to replace your obsolete outlet. Do not defeat the safety purpose of the grounding type plug.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the unit in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove unit covers. Qualified maintenance personnel must make component replacements and internal adjustments. Do not replace components with the power cord connected. Under certain conditions, dangerous voltages may exist even with the power cord removed. To avoid personal injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person capable of rendering first-aid resuscitation is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the unit.

DANGEROUS PROCEDURE WARNINGS

Warnings such as the example shown below precede potentially dangerous procedures throughout this document. Instructions contained in warnings must be followed.

WARNING

Dangerous voltages capable of causing death are present in this unit. Use extreme caution when handling, testing, or adjusting.

CAUTION

ELECTROSTATIC DISCHARGE (ESD) PRECAUTIONS

The following practices minimize possible damage to circuit boards resulting from electrostatic discharge or improper insertion.

- Keep circuit boards in their original packaging until ready for use.
- Avoid having plastic, vinyl, or Styrofoam in the work area.
- Wear an anti-static wrist strap.
- Discharge personal static before handling circuit boards.
- Remove and insert circuit boards with care.
- When removing circuit boards, handle only by non-conductive surfaces. Never touch open-edge connectors except at a static-free workstation.
- Minimize handling of circuit boards.
- Handle each circuit board by its edges.
- Do not slide circuit boards over any surface.
- Insert circuit boards with the proper orientation.
- Use static-shielded containers for storing and transporting circuit boards.

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Bedford, MA 01730-1413 USA
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www.lexicon.com

Customer Service
Telephone: 781-280-0300
Sales Fax: 781-280-0495

Service Fax: 781-280-0499

Product Shipments
16 Progress Road
Billerica, MA 01821-5730 USA

WARNING

These service instructions are only intended for use by qualified personnel. Do not perform any servicing other than that contained in these instructions unless qualified to do so. Refer to the Safety Summary on the previous page prior to performing any service.

A Harman International Company

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CHAPTER 1 – REQUIRED EQUIPMENT

Reference Document

Refer to the MC-8 User Guide-Lexicon P/N 070-15481.

Required Equipment

The following is a minimum suggested equipment list required to perform the proof of performance tests:

- High quality amplifier with RCA and XLR input connectors and volume control capabilities
- A pair of high quality speakers
- High quality video monitor with composite (RCA), S-video and component (RCA and BNC) input connections
- CD disc for use as a test audio source
- DVD disc for use as a test video source
- DAT Recorder for testing the digital output of the MC-8
- Variable AC power supply (2 amp minimum)
- Digital multimeter (DMM) 3.5 digits 0.5% or better accuracy
- Low Distortion Audio Oscillator with single-ended and balanced analog outputs, switchable 40kHz low-pass filter or band-pass (20-20kHz) filter, and output THD+N < 0.001%
- 100 MHz oscilloscope
- S/PDIF Digital Distortion Analyzer with coaxial and optical input
- S/PDIF Digital Function Generator with coaxial and optical output
- Low Distortion Audio Analyzer with switchable 30Hz high-pass filter or band-pass (20-20kHz) filter capable of measuring THD+N <0.01%
- DVD/CD player with RCA analog L/R outputs, digital coaxial outputs, optical outputs, and composite, S-video and component outputs
- (2) RS232 wrap around plugs (These are made by connecting pins 2 & 3 of a female DB9 connector)
- MC-8 remote control.

Required Cables

- Shielded audio cable with an RCA connector on one end and an appropriate connector on the opposite end for connection to a Low Distortion Audio Oscillator
- Shielded audio cable with an RCA connector on one end and an appropriate connector on the opposite end for connection to a Low Distortion Audio Analyzer
- Shielded (balanced) audio cable and a XLR female connector on one end and an appropriate connector on the opposite end for connection to a Low Distortion Analyzer
- (4) Shielded audio cables with RCA connectors on both ends

- (2) Shielded audio cables with a XLR male on one end and XLR female on the other
- Digital S/PDIF audio cable with RCA connectors on both ends
- Digital S/PDIF audio cable with optical connectors on both ends
- (2) Video cables with RCA connectors on both ends
- (2) Video cables with S-video connectors on both ends
- (2) Video cables with 3-wire component RCA connectors on both ends
- MC-8 AC power cord (see Chapter 7 for list of part numbers).

Required Tools

The following is a minimum suggested equipment list required for performing disassembly, assembly and repairs:

- Clean, antistatic, well-lit work area with grounding wrist strap
- Number 1 Phillips tip screwdriver (magnetic tip preferred)
- 14mm socket nut driver
- (2.5 mm) Hex Driver
- 3/16 Hollow nut driver
- Magnification glasses and lamp
- Surface Mount Technology (SMT) Soldering/Desoldering bench-top repair station.

CHAPTER 2 – GENERAL INFORMATION

Periodic Maintenance

Under normal conditions the MC-8 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, board assembly location, component location, price and HSG/Lexicon Part Number.

Replacement parts can be ordered from:

Harman Specialty Group
3 Oak Park Drive
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@harmanspecialtygroup.com
ATTN: Customer Service

Returning Units to HSG/Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with HSG/Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from HSG/Lexicon.

If HSG/Lexicon recommends that a MC-8 be returned for repair and you choose to return the unit to HSG/Lexicon for service, HSG/Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization number (on both the inside and outside of the package).

Please enclose a brief note describing any conversations with HSG/Lexicon personnel (indicate the name of the person at HSG/Lexicon) and give the name and daytime telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, remote controls, etc. with the unit, unless specifically requested to do so by HSG/Lexicon Customer Service personnel.

CHAPTER 3 – SPECIFICATIONS

Audio Input and Output Connectors

Analog Audio Inputs	8 stereo (RCA) *or* 5 stereo and one 5.1-channel *or* 2 stereo and two 5.1-channel connectors
Digital Audio Inputs	4 S/PDIF coaxial (RCA) and 4 S/PDIF optical connectors; coaxial and optical input connectors conform to IEC-958, S/PDIF standards
Sample Rates	44.1, 48, 88.2, 96kHz
Accepts	16-24 bits PCM audio, Dolby Digital, DTS, DTS-ES discrete data formats
Main Audio Outputs	8 unbalanced (RCA) and 8 balanced (XLR, MC-8 balanced only) connectors for Front L/R, Center, Sub, Side L/R and Rear L/R
Zone 2 Audio Outputs	1 unbalanced (RCA, variable output level) stereo connector, 1 balanced (XLR, variable output level, MC-8 balanced only) stereo connector, 1 S/PDIF coaxial (RCA) connector

Main Zone Audio Performance

A/D Conversion	24-bit, 96kHz, dual-bit ΔΣ architecture
D/A Conversion	24-bit, 44.1 to 192kHz, multi-bit ΔΣ architecture
Frequency Response*	10Hz to 20kHz, +0.05dB/-0.1dB, -0.5dB at 40kHz, reference 1kHz
THD + Noise*	Below 0.008% at 1kHz, maximum output level
Dynamic Range*	108dB minimum, 22kHz bandwidth
Signal-to-Noise Ratio*	108dB minimum, 22kHz bandwidth
Input Sensitivity	200mVrms (2Vrms for maximum output level) at 0dB input gain
Input Impedance	100kΩ in parallel with 150pF
Output Level	150mVrms typical, 6Vrms maximum (RCA connectors) 300mVrms typical, 12Vrms maximum (XLR connectors, MC-8 Balanced only) Maximum value with full-scale input signal and volume at +12dB
Output Impedance	100Ω in parallel with 150pF (RCA connectors), 50Ω in parallel with 150pF (XLR connectors, MC-8 Balanced only)

Zone 2 and Audio Performance

D/A Conversion	24-bit, 44.1 to 192kHz, multi-bit ΔΣ architecture
Frequency Response*	10Hz to 20kHz, +0.1dB/-0.25dB, -0.75dB at 40kHz, reference 1kHz
THD + Noise*	Below 0.005% at 1kHz, (maximum output level)
Dynamic Range*	103dB minimum, 108dB typical, 22kHz bandwidth
Signal-to-Noise Ratio*	103dB minimum, 108dB typical, 22kHz bandwidth
Input Sensitivity	200mVrms (4Vrms for maximum output level)
Input Impedance	100kΩ in parallel with 150pF
Output Level	200mVrms typical, 4Vrms maximum (RCA connectors), 400mVrms typical, 8Vrms maximum (XLR connectors), MC-8 Balanced only; maximum value with full-scale input signal and volume at 0dB
Output Impedance	100Ω in parallel with 150pF (RCA connectors), 50Ω in parallel with 150pF (XLR connectors, MC-8 Balanced only)

Video Input and Output Connectors

Video Inputs	5 composite (RCA), 5 S-video and 3 component video (RCA)
Video Outputs	2 composite (RCA), (1 monitor, 1 Zone 2), 2 S-video (1 monitor, 1 Zone2) and 1 component (BNC)

Composite and S-video Performance

Compatibility	NTSC, PAL and SECAM
Switching	Active
Output Level	1.0V peak-to-peak
Impedance	75Ω
Input Return Loss	>40dB
Differential Gain*	<0.5%
Differential Phase*	<0.5°
Bandwidth*	>25MHz
K Factor*	<0.3%
Gain*	±0.15dB

Signal-to-Noise Ratio*	>65dB
Frequency Response*	10Hz to 10MHz + 0.1/-0.3dB

Component Video Performance

Compatibility	3-Channel (Y/Pb/Pr), format-independent
Switching	Passive
Impedance	75Ω
Bandwidth	>150MHz
Insertion Loss*	<3dB

Microphone Input Connectors (For V2 and Higher Units)

Input	4 3.5 miniature phone jacks
Input Sensitivity	10mVrms (400mV maximum input level)
Input Impedance	20kΩ (accepts balanced or unbalanced input signals)

Other

Trigger Outputs	1 power on/off and 1 programmable connector on detachable screw terminals (+12 VDC, 0.5 amps each)
RS-232 Serial Input/Output	2 9-pin D-sub connectors
Power Requirements	90-250 VAC, 50-60Hz, 60W (universal line input), detachable power cord

MC-8 Dimensions & Weight

Height (with feet): 3.81 inches (97mm)

Width: 17.3 inches (440mm)

Depth: 14.85 inches (377mm)

Weight: 17lb (7.6kg)

MC-8 Balanced Dimensions & Weight

Height (with feet): 5.04 inches (128mm)

Width: 17.3 inches (440mm)

Depth: 14.85 inches (377mm)

Weight: 24lb (10.7kg)

Rack Mounting	Optional brackets are available for installation in a standard 19" equipment rack (2 rack units required for MC-8; 3 rack units for MC-8 Balanced)
Environment	**Operating Temp:** 0° to 35°C (32° to 95°F)
	Storage Temp: -30° to 75°C (-22° to 167°F)
	Relative Humidity: 95% maximum without condensation
Remote Control	Hand-held, backlit infrared remote control unit, preprogrammed & learning
	Requires two AA batteries (alkaline batteries recommended)

Specifications are subject to change without notice.

CHAPTER 4 – FUNCTIONAL VERIFICATION

PERFORMANCE VERIFICATION

This section describes a quick verification of the operation of the MC-8 and the integrity of its analog and digital audio signal paths. Tests that are specifically included for the MC-8 Balanced version can be omitted when testing an MC-8.

WARNING

Dangerous voltages capable of causing death are present in this unit. Use extreme caution when handling, testing, or adjusting. Always power down all equipment before breaking/making connections.

Initial Inspection

1. Inspect the MC-8 for obvious signs of physical abuse.
2. Verify that all switches operate smoothly.
3. With the power off for ten minutes and the AC cord disconnected, remove the MC-8 top cover using a hex wrench (2.5mm). Remove the 13 screws on the top cover of the unit to remove the cover.
4. Verify that all socketed ICs are correctly seated.
5. Verify that all cables are correctly installed and are securely fastened.
6. Check for burnt or obviously damaged components.
7. Put the top cover back on.
8. Power on the MC-8 using the main power switch on the back of the unit, and verify that the MC-8 runs through its Power On Diagnostics.
9. Check each of the front panel switches for smooth mechanical operation, verify each LED turns on and off when the associated switch is depressed, and that the display acknowledges each switch function.
10. Press each button on the remote and verify that the MC-8 is responding to all the remote commands.

FUNCTIONAL AUDIO I/O TESTS

The following tests verify the basic functions of the MC-8.

Power Supply Tests

The main power supply in the MC-8 has an operational range of 100-240VAC 50-60Hz, 60W. The following test is for North American line voltage of 120VAC.

Lethal voltages capable of causing death are present in this unit. In this procedure, testing will be performed with the top cover removed and the unit turned on. Due to risk of shock, do not remove the cover with the unit powered on.

Test:

1. Set the variable AC supply to 120 volts.
2. Verify that the MC-8 is powered off at its rear panel power switch.
3. Connect the power cord between the supply and the MC-8.
4. Remove the top cover.
5. Check for power supply shorts to ground.
6. Turn on the MC-8 using the rear main power switch.
7. Power on the unit at 120VAC.
8. Verify the current draw on the Variac does not exceed 0.6 amps.
9. Using a DMM, measure all the power supply rails as stated in the tables below, being sure to use the MC-8 chassis as ground.
10. Verify that all the voltages are within the tolerance range shown below.

Main Board

Supply Rail	Tolerance	Test Points
+5VD	4.75 - 5.25	Red wire at J45 behind front panel center at volume knob left to ground
Battery	≥ 2.5	Right side to the Left of U69, measure the top of the battery to ground
+15V	15.00 - 16.95	Yellow wire at J32 to ground
-15V	-14.25 - 15.75	Blue wire at J32 to ground
+5VAD	4.75 - 5.25	Red wire at J32 to ground
-5VA	-4.75 - 5.25	Gray wire at J32 to ground

Video Board

Supply Rail	Tolerance	Test Points
+5VAD	4.75 - 5.25	Red wire at J17 on Video board to ground
+5VA	4.75 - 5.25	Black wire at J17 on Video board to ground
-5VA	-4.75 - 5.25	Gray wire at J17 on Video board to ground

In order to properly test the MC-8 as described in this document, the MC-8 must be in Diagnostics mode. Perform the following procedure to enter the Diagnostics mode.

To enter Diagnostics mode:

1. Connect the video monitor to the composite output. This will allow full viewing of the Diagnostics menus of the MC-8.
2. Press and hold the front panel **Main VCR** and **Zone 2 VCR** buttons while powering up the MC-8 with the main power switch on the back of the unit.
3. When “LEXICON” appears on the display, release the buttons on the front panel.
4. The display on the MC-8 front panel will read “DIAGS MENU FUNCTIONAL TESTS.” The full Diagnostics Menu will be displayed on the monitor.

Analog Inputs To Main Zone Outputs Test

This test will verify the audio path between the RCA paired inputs labeled 1 to 8, to all analog outputs, both RCA and XLR.

Test:

1. Connect the low distortion oscillator output to the left and right audio inputs labeled 1 on the rear panel of the MC-8.
2. With the amplifier powered off, connect the RCA left and right front outputs of the MC-8 to the amplifier left and right inputs. Connect the outputs of the amplifier to the pair of speakers.
3. Using the remote control Menu ▼ arrow, scroll through the Diagnostics Menu and select the Audio I/O Tests.
4. In the Audio I/O Test menu, highlight Audio Input 1 Test, and then press the Menu ▶ arrow to engage the test. The MC-8 is now set to route audio from the left and right RCA inputs labeled 1 to all RCA analog outputs.
5. Power on the amplifier.
6. Slowly increase the volume on the amplifier to a comfortable listening level.
7. Sweep the oscillator from 20Hz to 20kHz.
8. Verify that clean, undistorted audio can be heard throughout the frequency sweep.
9. Power down the amplifier.
10. Repeat steps 5 through 7 for the remaining paired RCA outputs.

11. If testing an MC-8 Balanced unit, repeat the above procedure using XLR cables to connect the appropriate MC-8 XLR Main Zone outputs to the amplifier.
12. The above procedure should be repeated to test Analog inputs 2 through 8. To do this, repeat the procedure, changing the Input Test selected in step 4 to the next appropriate Input. The oscillator outputs will need to be moved to the appropriate MC-8 Input, corresponding to the Input selected in the Audio I/O Test Menu.

Digital Inputs to Main Zone Outputs Test

This test will verify the audio path between the S/PDIF coaxial and optical digital inputs labeled (1 to 4), to all analog outputs, both RCA and XLR.

***Note**:*
This test requires the use of a DVD/CD player as a source. The tests to follow will be run using a PCM signal at a 44.1kHz sample rate.

Test:

1. Connect the S/PDIF coaxial digital output of the DVD/CD player to the S/PDIF coaxial digital input 1 on the rear of the MC-8.
2. With the amplifier off, connect the RCA left and right front outputs of the MC-8 to the amplifier left and right inputs. Connect the outputs of the amplifier to a pair of speakers.
3. Using the remote control Menu ▼ arrow, scroll through the Diagnostic Menu and select the Audio I/O Tests.
4. In the Audio I/O Test Menu, highlight S/PDIF Input CX 1 Test then press the Menu ▶ arrow to engage the test. The MC-8 is now set to route digital audio from the S/PDIF coaxial digital input 1 to all the RCA analog outputs.
5. Insert a CD and press play on the player.
6. Power on the amplifier.
7. Slowly increase the volume on the amplifier to a comfortable listening level.
8. Verify that clean, undistorted audio can be heard.
9. Stop the DVD player and power down the amplifier.
10. Repeat steps 2 through 7 for the remaining paired RCA outputs.
11. If testing an MC-8 Balanced unit, repeat the above procedure using XLR cables to connect the appropriate MC-8 XLR Main Zone Outputs to the amplifier.
12. The above procedure should be repeated to test digital S/PDIF Inputs 2 through 4, as well as optical Inputs labeled 1 to 4. To do this repeat the procedure, changing the Input test selected in step 4 to the next appropriate Input. The DVD output will need to be moved to the appropriate MC-8 Input, corresponding to the Input selected in the Audio I/O Test Menu. When testing the optical inputs, be sure to use the appropriate digital cable.

AUDIO PERFORMANCE VERIFICATION

Performing these tests assures that the audio signal paths in the MC-8 meet published specifications. These tests will verify the performance specifications of the A/D and D/A circuitry: gain, frequency response, THD+N, S/N ratio, and dynamic range (when applicable) of each channel.

Analog Audio Inputs To Main Zone RCA Output Tests

These tests will verify the specifications of the Main Zone RCA output channels.

Setup:

1. Connect an audio cable between the output of the Low Distortion Oscillator and the MC-8 left RCA input 1.
2. Connect an audio cable between the left front RCA output of the MC-8 and the input of the Distortion Analyzer.
3. Using the MC-8 Remote Control Menu ▼ arrow, scroll through the Diagnostic Menu and select the Audio I/O Tests.
4. In the Audio I/O Test Menu, highlight Audio Input 1 Test, and then press the Menu ▶ arrow to engage the test. The MC-8 is now set to route audio from the left and right RCA inputs labeled 1 to all RCA analog outputs.

Gain Test (GAIN) Test:

1. Apply a 997Hz signal @ + 4Vrms to Analog input labeled 1.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filter not required for Gain Test).
4. Verify that the output level measurement from the MC-8 is between the range of +6.60Vrms and +8.90Vrms. Note this level.

Total Harmonic Distortion + Noise Test (THD+N):

1. Adjust the scale on the Distortion Analyzer to measure 0.001% THD+N and turn on the 40kHz low pass or audio band pass filter.
2. Sweep the oscillator frequency from 20Hz to 2kHz, and 8kHz to 40kHz.
3. Verify that the THD+N measured on the Analyzer is less than 0.01% (20Hz to 2kHz), and 0.02% (8kHz to 40kHz).

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure +4Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check Frequency Response for the MC-8.
3. Turn the filter on the analyzer off.
4. Sweep the oscillator frequency from 10Hz to 40kHz.
5. Verify the signal levels are +0.05dBr to –0.15dBr 10Hz-20kHz, and +0.05dBr to –0.50dBr 20kHz-40kHz of reference level over the entire sweep.

Signal to Noise Test (SNR):

1. Using the 0dBr from step 2 of the Frequency Response Test, turn off the oscillator and verify a noise level measurement <-108dBr.
2. Swap cables from the left RCA input 1 to the right RCA input 1 and the left front RCA output to the right front RCA output. Repeat the GAIN, THD+N, FREQ and SNR tests for the remaining Main Zone RCA Outputs.

Digital Inputs to Main Zone RCA Output Tests

Having tested all analog-to-analog specifications in the previous tests, it is now necessary to verify that all the digital inputs pass specifications. These tests will verify the specifications of all digital inputs to the front left and right RCA outputs.

Setup:

1. Connect a digital audio cable from the output of the Digital Function Generator to S/PDIF coaxial input 1 on the rear of the MC-8.
2. Connect an audio cable between the left front RCA output of the MC-8 and the input of the Analog Distortion Analyzer.
3. Using the remote control Menu ▼ arrow, scroll through the Diagnostic Menu and select the Audio I/O Tests.
4. In the Audio I/O Test Menu, highlight S/PDIF Input CX number 1 Test then press the Menu ▶ arrow to engage the test. The MC-8 is now set to pass digital audio from the S/PDIF coaxial RCA input 1 to the front left and right RCA output.

Gain Test (GAIN):

1. Apply a 997Hz signal @ + 0.00dBFS (1Vrms) to S/PDIF coaxial input labeled 1.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filters not required for Gain Test).
4. Verify that the output level measurement from the MC-8 is between the range of +3.73Vrms and +4.47Vrms. Note this level.

Total Harmonic Distortion + Noise Test (THD+N):

1. Adjust the scale on the Distortion Analyzer to measure 0.001% THD+N and turn on the 40kHz low pass or audio band pass filter.
2. Sweep the oscillator frequency from 20Hz to 2kHz, and 8kHz to 40kHz.
3. Verify that the THD+N measured on the Analyzer is less than 0.005% (20Hz to 2kHz), and 0.0175% (8kHz to 40kHz).

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check Frequency Response for the MC-8.
3. Turn the filter on the analyzer off.
4. Sweep the oscillator frequency from 10Hz to 40kHz.
5. Verify the signal levels are +0.05dBr to –0.10dBr 10Hz-20kHz, and +0.05dBr to –0.50dBr 20kHz-40kHz of reference level over the entire sweep. Note these levels.

Dynamic Range Test (DYNRNG):

Using steps 1-3 of the Gain Test, set the oscillator to -60dBFS and verify a THD+N level measurement <-108dBr.

Test the remaining inputs:

Use the GAIN, THD, FREQ and DYNRNG tests described above to test the remaining digital inputs (three coaxial and four optical). When testing the optical inputs, be sure to use the appropriate digital cable.

Digital Inputs to Main Zone XLR Outputs Test

***Note**:*
This test is for MC-8 Balanced units only.

Setup:

1. Connect a digital audio cable from the output of the Digital Function Generator to S/PDIF coaxial input 1 on the rear of the MC-8B.
2. Connect an audio cable between the left front XLR output of the MC-8B and the input of the Analog Distortion Analyzer.
3. Using the MC-8B Remote Control Menu ▼ arrow, scroll through the Diagnostic Menu and select the Audio I/O Tests.
4. In the Audio I/O Test Menu, highlight S/PDIF Input CX number 1 Test then press the Menu ▶ arrow to engage the test. The MC-8B is now set to pass digital audio from the S/PDIF coaxial RCA input 1 to the front left and right XLR output.

Gain Test (GAIN):

1. Apply a 997Hz signal @ +0.00dBFS to S/PDIF coaxial input 1.
2. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
3. Turn all the filters off on the Analyzer (Filter not required for Gain Test).
4. Verify that the output level measurement from the MC-8B is between the range of +7.43Vrms and +8.83Vrms. Note this level.

Total Harmonic Distortion + Noise Test (THD+N):

1. Adjust the scale on the Distortion Analyzer to measure 0.001% THD+N and turn on the 40kHz low pass or audio band pass filter.
2. Sweep the oscillator frequency from 20Hz to 1kHz, and 5kHz to 40kHz.
3. Verify that the THD+N measured on the Analyzer is less than 0.005% (20Hz to 1kHz), and 0.02% (5kHz to 40kHz).

Frequency Response Test (FREQ):

1. Set the scale on the Distortion Analyzer to measure +8Vrms signal level.
2. Using the output level from step 4 of the Gain Test, set the Distortion Analyzer for a 0dB reference to check Frequency Response for the MC-8B.
3. Turn the filter on the analyzer off.
4. Sweep the oscillator frequency from 10Hz to 40kHz.
5. Verify the signal levels are +0.10dBr to –0.25dBr 10Hz-20kHz, and +0.10dBr to –0.75dBr 20kHz-40kHz of reference level over the entire sweep. Note these levels.

Dynamic Range (DYNRNG):

Using steps 1-3 of the Gain Test, set the oscillator to -60dBFS and verify a THD+N level measurement <-108dBr.

Test the remaining inputs:

Use the GAIN, THD, FREQ and DYNRNG tests described above to test the remaining digital inputs (three coaxial and four optical). When testing the optical inputs, be sure to use the appropriate digital cable.

VIDEO INPUT/OUTPUT TESTS

These tests will verify that all thirteen video inputs and five video outputs pass video. There are three different video paths to be tested in the MC-8: composite, S-video, and component. Composite and S-video paths each have five inputs and two outputs. Component paths have three inputs and one output. The following tests will verify that the MC-8 is passing clear, undistorted video. It is not necessary to enter the Extended Diagnostics as was done in the audio tests.

Composite Video Input to Composite Video Outputs Test

This test will verify the composite video switching function of the MC-8.

Setup:

1. Connect the composite video output from the DVD player to the MC-8's composite video input 1.
2. Connect the main composite output of the MC-8 to the composite input of the video monitor.
3. Turn on the DVD player, monitor, and the MC-8.
4. The monitor should display a blue screen.
5. Press the remote **DVD1** button to select DVD-1 as the input for testing the video paths.
6. Press the Menu ▸ arrow. The MC-8 Main Menu will be displayed.
7. With the Menu ▾ arrow, scroll down to SETUP, then select by pressing the Menu ▸ arrow.
8. The Setup Menu will appear and Inputs at the top will be highlighted.
9. Press the Menu ▸ arrow again.
10. The display will read DVD1 Input Setup.
11. Press the Menu ▸ arrow. The DVD1 Menu will now be displayed.
12. Using the Menu ▾ arrow, scroll down to the Video In parameter and select it by pressing the Menu ▸ arrow.
13. Using the Menu ▾ arrow scroll to the video input Composite-1.
14. Press the Menu ▸ arrow to select video input Composite-1. This will assign the Composite -1 Video input to the main composite output of the MC-8.
15. Press the remote **OSD** button to turn off the onscreen video information from the MC-8 and allow viewing of the video from the DVD player.
16. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor.
3. Pause the DVD player.
4. To test the second composite output, switch the composite monitor output cable on the rear of the MC-8 to the composite Zone 2 video output then repeat the procedure.
5. The setup and test procedure should be repeated to test composite video inputs labeled 2 through 5. To do this, repeat the procedure, changing the Input Test selected in step 14 to the appropriate Input.

S-video Inputs to S-video Outputs Test

This test will verify the S-video switching function of the MC-8.

Setup:

1. Connect the S-video output from the DVD player to the MC-8 S-video input 1.
2. Connect the main S-video output of the MC-8 to the S-video input of the video monitor.
3. Turn on the DVD player, monitor, and the MC-8.
4. The monitor should display a blue screen.
5. Press the remote **DVD1** button to select this as the input for testing the video paths.
6. Press the Menu ▸ arrow. The Main Menu should appear on the screen.
7. With the Menu ▾ arrow, scroll down to Setup, and then select it by pressing the menu ▸ arrow.
8. The Setup Menu will appear and the Inputs at the top will be highlighted.
9. Press the Menu ▸ arrow again.
10. The display will read Input Setup DVD1.
11. Press the Menu ▸ arrow. The display on the MC-8 will now be at the top on the DVD1 Menu.
12. Using the Menu ▾ arrow, scroll down to the Video In parameter and select it by pressing the Menu ▸ arrow.
13. Using the Menu ▾ arrow, scroll to the video input S-video-1.
14. Press the Menu ▸ arrow to select the S-video-1 input. This will assign the S-video-1 input jack to the Main Zone S-video output jack of the MC-8.
15. Press the remote **OSD** button. This will turn off the onscreen video information from the MC-8 and allow viewing of the video from the DVD player.
16. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor screen.
3. Pause the DVD player.
4. To test the Zone 2 S-video output, switch the S-video monitor output cable on the back of the MC-8 to the Zone 2 S-video output then repeat the procedure.
5. The above procedure should be repeated to test S-video inputs labeled 2 through 5. To do this, repeat the procedure, changing the input selected in step 14 to the appropriate input.

Component Video Input to Component Video Output Test

This test will verify the component video switching function of the MC-8.

Setup:

1. Connect the component video output from the DVD player to the MC-8 component video input 1.
2. Connect the main component output of the MC-8 to the component input of the video monitor.
3. Turn on the DVD player, monitor, and the MC-8.
4. The monitor should display a blue screen.
5. Press the remote **DVD1** button to select this as the input for testing the video paths.
6. Press the Menu ▸ arrow. The Main Menu should appear on the display.
7. Using the Menu ▾ arrow, scroll down to Setup, then select by pressing the Menu ▸ arrow.
8. The Setup Menu will appear and the inputs at the top will be highlighted.
9. Press the Menu ▸ arrow again.
10. The display will read Input Setup DVD1.
11. Press the Menu ▸ arrow. The display on the MC-8 will now be at the top of the DVD1 Menu.
12. Using the Menu ▾ arrow, scroll down to the Component In parameter and select it by pressing the Menu ▸ arrow.
13. Press the Menu ▾ arrow to select the Component1 input. This will assign the component 1 video input jack to the main component video output jack of the MC-8.
14. Press the remote **OSD** button. This will turn off the on-screen video information from the MC-8 and allow viewing of the video from the DVD player.
15. The video path is now set for testing.

Test:

1. Load a disc into the DVD player and press play.
2. Verify a clean undistorted picture appears on the monitor screen.
3. Pause the DVD player.
4. The above procedure should be repeated to test the remaining two component Video inputs. To do this, repeat the procedure, changing the Input selected in step 14 to the appropriate Input.

LEXICON AUDIO PRECISION ATE SUMMARY

This chart, which begins on the next page, represents a summary of Audio Precision test settings and parameters used by Lexicon in production testing of all MC-8 products. This chart as well as the MC-8 ATE summary is provided as a reference and supplement to bench test settings found in the rest of the Performance Verification section.

D-D Tests		Digital Generator						Digital Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
DIG_ZONE_COAX1_IN_96k_TO_DIG_ZONE_COAX_OUT																							
DIG_ZONE_COAX1_IN_96k_TO_DIG_ZONE_COAX_OUT_GAIN		-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBFS	Level	-0.999	-0.90	-1.10	n/a	n/a	<10 - Fs/2	n/a	n/a	n/a	n/a	11	External	96000	Analog
DIG_ZONE_COAX1_IN_96k_TO_DIG_ZONE_COAX_OUT_THD		-1dBFS	-1dBFS	10-40k	n/a	n/a	n/a	dBFS	THD+N	-144.00	-140.00	-999.00	n/a	n/a	<10Hz->20kHz LP	n/a	n/a	n/a	n/a	11	External	96000	Analog

D-A Tests		Digital Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT_FREQ		-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	20-2k/8k-40k	n/a	n/a	n/a	%	THD+N	<.003/.0075	.005/.0175	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT_XTALK		-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-90.00	-80.00	-150.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_88k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX1_IN_88k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	88200	Digital
DIG_ZONE_COAX1_IN_88k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	88200	Digital
DIG_ZONE_COAX1_IN_88k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External	88200	Digital
DIG_ZONE_COAX1_IN_48k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX1_IN_48k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	48000	Digital
DIG_ZONE_COAX1_IN_48k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	48000	Digital
DIG_ZONE_COAX1_IN_48k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-106.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External		Digital
DIG_ZONE_COAX1_IN_44k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX1_IN_44k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	44100	Digital
DIG_ZONE_COAX1_IN_44k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	44100	Digital
DIG_ZONE_COAX1_IN_44k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-106.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External	44100	Digital
DIG_ZONE_COAX2_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX2_IN_44k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_COAX2_IN_44k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_COAX2_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_COAX3_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX3_IN_44k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_COAX3_IN_44k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_COAX3_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_COAX4_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_COAX4_IN_44k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_COAX4_IN_44k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_COAX4_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_OPT1_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_OPT1_IN_96k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_OPT1_IN_96k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_OPT1_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	11	External	96000	Digital
DIG_ZONE_OPT2_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_OPT2_IN_96k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_OPT2_IN_96k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_OPT2_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	12	External	96000	Digital
DIG_ZONE_OPT3_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_OPT3_IN_96k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_OPT3_IN_96k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_OPT3_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	13	External	96000	Digital
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT																							
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+4.10	+4.47	+3.73	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_THD		-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-103.00	-140.00	None	100k	<10 - 22k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_OUTLEVEL_MUTE																							
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_OUTLEVEL_MUTE		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-103.00	-99.00	-1001.00	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_RELAY_MUTE																							
DIG_ZONE_OPT4_IN_96k_TO_ANLG_ZONE_OUT_RELAY_MUTE		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-125.00	-120.00	-1001.00	40kHz LP	100k	<10 - >500k	9	10	n/a	n/a	14	External	96000	Digital

DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_GAIN	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_FREQ	3	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.30	+0.05	-0.10/-0.50	None	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_THD	3	-1.00dBFS	-1.00dBFS	20-2k/8k-40k	n/a	n/a	n/a	%	THD+N	<.003/.010	.005/.0175	.0002	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_XTALK	3	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-90.00	-80.00	-150.00	None	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_DYNRNG	3	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital

D-A Tests		Digital Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_OUTLEVEL_MUTE																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_OUTLEVEL_MUTE	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-104.00	-100.00	1001.00	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_RELAY_MUTE																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_RELAY_MUTE	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-125.00	-120.00	1001.00	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_CLKRNG																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_CLKRNG	4	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	>-92.00	-82.00	-105.00	None	100k	<10 - 22k	1	n/a	n/a	n/a	11	External	87.3K-89.1K	Digital
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT_GAIN	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	88200	Digital
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT_THD	3	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	88200	Digital
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT_DYNRNG	3	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	88200	Digital
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT_CLKRNG																							
DIG_MAIN_COAX1_IN_88K_TO_ANLG_MAIN_OUT_CLKRNG	4	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	>-92.00	-82.00	-105.00	None	100k	<10 - 22k	1	n/a	n/a	n/a	11	External	97K-95K	Digital
DIG_MAIN_COAX1_IN_48K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_COAX1_IN_48K_TO_ANLG_MAIN_OUT_GAIN	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	48000	Digital
DIG_MAIN_COAX1_IN_48K_TO_ANLG_MAIN_OUT_THD	3	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	48000	Digital
DIG_MAIN_COAX1_IN_48K_TO_ANLG_MAIN_OUT_DYNRNG	3	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	48000	Digital
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_OUT																							
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_OUT_GAIN	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	44100	Digital
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_OUT_THD	3	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	44100	Digital
DIG_MAIN_COAX1_IN_44K_TO_ANLG_MAIN_OUT_DYNRNG	3	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	44100	Digital

D-A XLR Tests *(MC-8B ONLY)*		Digital Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT																							
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_GAIN		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_FREQ		-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.15/-0.60	+0.10	-0.25/-0.75	None	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_THD		-1.00dBFS	-1.00dBFS	20-1k/5k-40k	n/a	n/a	n/a	%	THD+N	<.003/.075	.005/.020	.0002	40kHz LP	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_XTALK		-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-88.00	-80.00	-150.00	None	100k	<10 - 22k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_DYNRNG		-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-105.00	-140.00	None	100k	<10 - 22k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_600																							
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_GAIN_600		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+6.85	+7.50	+6.30	40kHz LP	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_THD_600		-1.00dBFS	-1.00dBFS	100	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_RELAY_MUTE																							
DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_OUT_RELAY_MUTE		+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-135.00	-120.00	-1001.00	40kHz LP	100k	<10 - >500k	21	22	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_GAIN	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+16.10	+17.60	+14.80	40kHz LP	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_FREQ	3	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.05/-0.25	+0.05	-0.1/-0.5	None	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_THD	3	-1.00dBFS	-1.00dBFS	20-1k/5k-40k	n/a	n/a	n/a	%	THD+N	<.003/.010	.005/.020	.0002	40kHz LP	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_XTALK	3	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-83.00	-80.00	-150.00	None	100k	<10 - 22k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_DYNRNG	3	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	None	100k	<10 - 22k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_600																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_GAIN_600	3	-3.00dBFS	-3.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+9.65	+10.63	+8.93	40kHz LP	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_THD_600	3	-3.00dBFS	-3.00dBFS	100	n/a	n/a	n/a	%	THD+N	<.003	.005	.0002	40kHz LP	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_RELAY_MUTE																							
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_OUT_RELAY_MUTE	3	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-140.00	-120.00	-1001.00	40kHz LP	100k	<10 - >500k	13,15,17,19	14,16,18,20	n/a	n/a	11	External	96000	Digital

A-A Tests		Analog Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	1	13	n/a	Internal	96000	Analog
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	1	13	n/a	Internal	96000	Analog
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	1	13	n/a	Internal	96000	Analog
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	1	13	n/a	Internal	96000	Analog
ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	1	13	n/a	Internal	96000	Analog
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	2	14	n/a	Internal	96000	Analog
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	2	14	n/a	Internal	96000	Analog
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	2	14	n/a	Internal	96000	Analog
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	2	14	n/a	Internal	96000	Analog
ANLG_ZONE_IN2_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	2	14	n/a	Internal	96000	Analog

A-A Tests		Analog Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	3	15	n/a	Internal	96000	Analog
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	3	15	n/a	Internal	96000	Analog
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	3	15	n/a	Internal	96000	Analog
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	3	15	n/a	Internal	96000	Analog
ANLG_ZONE_IN3_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	3	15	n/a	Internal	96000	Analog
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	4	16	n/a	Internal	96000	Analog
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	4	16	n/a	Internal	96000	Analog
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	4	16	n/a	Internal	96000	Analog
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	4	16	n/a	Internal	96000	Analog
ANLG_ZONE_IN4_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	4	16	n/a	Internal	96000	Analog
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	5	17	n/a	Internal	96000	Analog
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	5	17	n/a	Internal	96000	Analog
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	5	17	n/a	Internal	96000	Analog
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	5	17	n/a	Internal	96000	Analog
ANLG_ZONE_IN5_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	5	17	n/a	Internal	96000	Analog
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	6	18	n/a	Internal	96000	Analog
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	6	18	n/a	Internal	96000	Analog
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	6	18	n/a	Internal	96000	Analog
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	6	18	n/a	Internal	96000	Analog
ANLG_ZONE_IN6_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	6	18	n/a	Internal	96000	Analog
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	7	19	n/a	Internal	96000	Analog
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	7	19	n/a	Internal	96000	Analog
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	7	19	n/a	Internal	96000	Analog
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	7	19	n/a	Internal	96000	Analog
ANLG_ZONE_IN7_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	7	19	n/a	Internal	96000	Analog
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT																							
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT_GAIN		4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.30	+3.70	40kHz LP	100k	<10 - >500k	9	10	8	20	n/a	Internal	96000	Analog
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT_FREQ		2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	9	10	8	20	n/a	Internal	96000	Analog
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT_THD		4.0Vrms	4.0Vrms	20-40k	20	Unbal	Float	%	THD+N	<.010	.015	.00005	40kHz LP	100k	<10 - >500k	9	10	8	20	n/a	Internal	96000	Analog
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT_XTALK		4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-115.00	-100.00	-150.00	None	100k	<10 - >22k	9	10	8	20	n/a	Internal	96000	Analog
ANLG_ZONE_IN8_96K_TO_ANLG_ZONE_DIR_OUT_SNR		OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-95.00	-140.00	None	100k	<10 - >22k	9	10	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	1	13	n/a	Internal	96000	Analog
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	1	13	n/a	Internal	96000	Analog
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	1	13	n/a	Internal	96000	Analog
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	1	13	n/a	Internal	96000	Analog
ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	1	13	n/a	Internal	96000	Analog
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	2	14	n/a	Internal	96000	Analog
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	2	14	n/a	Internal	96000	Analog
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	2	14	n/a	Internal	96000	Analog
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	2	14	n/a	Internal	96000	Analog
ANLG_MAIN_IN2_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	2	14	n/a	Internal	96000	Analog
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	3	15	n/a	Internal	96000	Analog
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	3	15	n/a	Internal	96000	Analog
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	3	15	n/a	Internal	96000	Analog
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	3	15	n/a	Internal	96000	Analog
ANLG_MAIN_IN3_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	3	15	n/a	Internal	96000	Analog
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	4	16	n/a	Internal	96000	Analog
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	4	16	n/a	Internal	96000	Analog
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	4	16	n/a	Internal	96000	Analog
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	4	16	n/a	Internal	96000	Analog
ANLG_MAIN_IN4_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	4	16	n/a	Internal	96000	Analog
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	5	17	n/a	Internal	96000	Analog
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	5	17	n/a	Internal	96000	Analog
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	5	17	n/a	Internal	96000	Analog
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	5	17	n/a	Internal	96000	Analog
ANLG_MAIN_IN5_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	5	17	n/a	Internal	96000	Analog

A-A Tests		Analog Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	6	18	n/a	Internal	96000	Analog
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	6	18	n/a	Internal	96000	Analog
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	6	18	n/a	Internal	96000	Analog
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	6	18	n/a	Internal	96000	Analog
ANLG_MAIN_IN6_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	6	18	n/a	Internal	96000	Analog
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	7	19	n/a	Internal	96000	Analog
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	7	19	n/a	Internal	96000	Analog
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	7	19	n/a	Internal	96000	Analog
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	7	19	n/a	Internal	96000	Analog
ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	7	19	n/a	Internal	96000	Analog
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT																							
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT_GAIN	3	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.80	+8.90	+6.60	40kHz LP	100k	<10 - >500k	1	2	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.05/-0.25	+0.05	-0.15/-0.50	None	100k	<10 - >500k	1	2	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT_THD	3	4.0Vrms	4.0Vrms	20-2k/8k-40k	20	Unbal	Float	%	THD+N	<.005/.010	.010/.020	.00005	40kHz LP	100k	<10 - >500k	1	2	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-80.00	-150.00	None	100k	<10 - >22k	1	2	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-99.00	-97.00	-140.00	None	100k	<10 - >22k	1	2	8	20	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT																							
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_GAIN	3	4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.15	+3.85	40kHz LP	100k	<10 - >500k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.03	+0.05	-0.25	None	100k	<10 - >500k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_THD	3	4.0Vrms	4.0Vrms	20-5k/10k-40k	20	Unbal	Float	%	THD+N	<.01/.015	.010/.020	.00005	40kHz LP	100k	<10 - >500k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-104	-95.00	-150.00	None	100k	<10 - >22k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-100.00	-140.00	None	100k	<10 - >22k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX																							
ANLG_MAIN_IN345_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX	2 & 3	OFF	OFF	997	20	Unbal	Float	Vrms	Level	-80.00	-70.00	-140.00	40kHz LP	100k	<10 - >500k	3,4,5,5	15,16,17,17	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT																							
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_GAIN	3	4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+4.00	+4.15	+3.85	40kHz LP	100k	<10 - >500k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_FREQ	3	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.03	+0.05	-0.25	None	100k	<10 - >500k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_THD	3	4.0Vrms	4.0Vrms	20-5k/10k-40k	20	Unbal	Float	%	THD+N	<.01/.015	.010/.020	.00005	40kHz LP	100k	<10 - >500k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_XTALK	3	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-104	-95.00	150.00	None	100k	<10 - >22k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_SNR	3	OFF	OFF	997	20	Unbal	Float	dBr	Level	-108.00	-100.00	-140.00	None	100k	<10 - >22k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX																							
ANLG_MAIN_IN678_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX	2 & 3	OFF	OFF	997	20	Unbal	Float	Vrms	Level	-80.00	-70.00	-140.00	40kHz LP	100k	<10 - >500k	6,7,8,8	18,19,20,20	1,3,5,7	2,4,6,8	n/a	Internal	96000	Analog

D-A DSP Tests		Digital Generator						Analog Analyzer								Switcher Module				MC-8/B Setup			
Test Name	See Note:	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	A In	B In	A Out	B Out	Midiman PGM #:	Clock Source	Sample Rate	Audio Source
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP																							
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP_GAIN	3 & 5	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.10	+8.83	+7.43	40kHz LP	100k	<10 - >500k	1,3,5,7	2,4,6,8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP_THD	3 & 5	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	1,3,5,7	2,4,6,8	n/a	n/a	11	External	96000	Digital
DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_DSP_DYNRNG	3 & 5	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	1, 3, 5, 7	2, 4, 6, 8	n/a	n/a	11	External	96000	Digital

Notes:

1. The Analog Zone Direct Input paths are selected at the MUX while the Zone D/A converter is being driven with a -1dBFS Digital Input from COAX1.
2. The Analog Main Direct Input paths are selected at the MUX while the Main D/A converters are being driven with a -1dBFS Digital Input from COAX1.
3. The Audio Precision Switcher channels are selected during the Audio ATE macro.
4. The CLKRNG Tests are used to verify the operation of the PLL circuitry.
5. The DSP Tests are used to verify the operation of the Decoder and DSP Boards.

CHAPTER 5 – TROUBLESHOOTING

This chapter contains a complete description of the diagnostic tests for the MC-8/MC-8 Balanced (MC8/B). The diagnostics in the MC8/B are used to verify functionality of the unit and to aid in troubleshooting defective units. Familiarity is assumed with the MC8/B BOM structure, all applicable assembly drawings, FAT process, and Audio ATE processes.

Diagnostic Categories

There are two types of diagnostics in the MC8/B: power-on and extended. The extended diagnostics contain the tests that are used by manufacturing personnel to verify functionality and by repair personnel to aid in troubleshooting. The entire set of power-on diagnostics is executed every time a unit is powered on using the rear panel power switch. The power-on diagnostic tests can be run individually in the extended diagnostics. The extended diagnostics also contain additional tests used to verify all the front panel controls, infrared communications, audio and video performance, etc. The troubleshooting or repair diagnostics are used to troubleshoot an MC8/B if any test fails.

Power On Modes

There are two power-on modes available. Power on via the rear panel power switch, or by bringing the unit out of standby mode. The power-on diagnostics are executed every time the rear panel power switch is switched on. When an MC8/B is operating, if the front panel Standby button is pressed, the unit goes into low power/Standby mode. Pressing any front panel button or any remote key will bring the MC8/B out of Standby mode. No diagnostics are run when the unit is brought out of Standby.

Diagnostics User Interface

Various combinations of button pushes are used to control diagnostic activity. The table below summarizes the options available, followed by more detailed descriptions.

Action	Buttons to be Held
Enter Diagnostics	MAIN VCR & ZONE2 VCR
Skip Power-On Diagnostics	MAIN AUX & ZONE2 AUX
Jump to Extended Diagnostics	MAIN OFF & ZONE2 OFF
Attempt to Run the Next Diagnostic Test	MAIN TV & ZONE2 TV

To Enter Extended Diagnostics:

Press and hold the front panel **MAIN VCR and ZONE 2 VCR** buttons when powering on a MC8/B.

To Enter Extended Diagnostics via Serial Debug Port:

Enter the debug program by typing “debug” when connected to the serial port. The debug program is case sensitive.

In addition, the extended diagnostics can be entered by sending “ed”, (for extended diagnostics), to the unit via the serial debug port during the first ten seconds after powering on the unit.

To skip Power On Diagnostics:

Press and hold the front panel **MAIN AUX** and **ZONE2 AUX** buttons. This will cause the unit to skip the power-on diagnostics and go immediately to the operating system. Immediately after sufficient testing is performed to verify the system can boot, (the Z180 CPU, EPROM, Z80 SRAM, FPGAs loaded, VFD etc.), the diagnostics check to see if MAIN AUX and the ZONE2 AUX buttons are being pressed together. If they are, the unit will attempt to skip the rest of the power up diagnostic tests and jump to the operating system.

To bridge to Extended Diagnostics after a failure occurs:

Press and hold the front panel **MAIN OFF** and **ZONE2 OFF** buttons. This will cause the unit to bridge to the extended diagnostics. After a failure the unit will attempt to display, on the VFD, and the front panel LEDs, the failed test number, and loop on the failing test. If the Z180 CPU and support circuitry is not working the unit will not attempt to read any front panel switches.

To execute the next Diagnostic Test after a failure occurs:

Press and hold the front-panel **MAIN TV** and **ZONE2 TV** buttons. This will cause the MC8/B to attempt to execute the next power on diagnostic step. If a failure occurs, the MC8/B attempts to enter a test loop to keep the signal lines active as an aid in debugging the failure. At the end of each successive loop, the diagnostics will check to see if the **MAIN TV** and **ZONE 2 TV** buttons are being held. Depending on the length of the test, the amount of time required pressing and holding the buttons will vary.

DIAGNOSTIC REPORTING

All diagnostic functionality is reported to the Vacuum Fluorescent Display (VFD) and to the front panel LEDs. They report on what test is being executed, and if the test passed or failed. The LEDs are used to report diagnostic status in the event that the VFD is not functioning.

Diagnostic status and data is also available on an external PC or a terminal, via the serial debug port located at the D9 connector labeled RS232 2 on the rear panel. The D9 connector labeled RS232 1 is used for updating the flash memory. In the event a diagnostic failure occurs for those diagnostic tests that report to the error log, additional failure information, such as data sent, data received, address location, etc., is listed in the error log. For example, Sharc SRAM failures are not reported to the error log. The error log can be viewed via the VFD, or it can be sent to the serial debug port.

Vacuum Fluorescent Display (VFD)

The VFD is the primary source of information during diagnostics. The exact display information will depend on the test(s) being executed. When an individual diagnostic test is executed, the VFD will display the name of that test. Groups of tests, such as the power-on diagnostics or the burn-in loop, have a generic message on the top line of the VFD. For example, “DIAGNOSTIC TESTS” is on the VFD while the power-on diagnostics is being run. An E followed by a number indicates a test failure message.

Front Panel LEDs

The top row of the front panel LEDs is also used to display diagnostic status. The LEDs are used in binary format with the Zone 2 VCR LED as the LSB and the Main DVD 1 LED as the MSB. Running test number 1 would illuminate the Zone 2 VCR LED only with all the others off. Running test number 2 would illuminate the Zone 2 Sat LED only with all others off. Running test number 3 would illuminate the Zone 2 SAT and the Zone 2 VCR LEDs together with all others off, etc.

If a failure occurs, the MUTE LED is illuminated to indicate the test failure, and the LEDs indicating which test was running when the failure occurred will also continue to be illuminated. The diagnostics will attempt to continuously execute the failed test, a test loop, to keep the signal lines active as an aid in debugging the failure.

Serial Debug Port

The Serial Debug Port is available to provide diagnostic status to be viewed on an external PC from the D9 connector labeled RS232 2. Using a terminal or a PC running a terminal program connected to RS232 2 the progress of the diagnostics can be monitored and test failure information is reported. Also, there is an error log can be dumped to the serial debug port while in extended diagnostics. The serial protocol is 19,200bps, 8, N, 1, (8 data bits, no parity and 1 stop bit).

Serial Debug Cable

The cable required to connect the RS232 2 serial debug port to the computer is a straight-through serial interface cable. A null modem adapter or cable should not be used. The MC8/B RS232 connector on the rear panel is a D9 female; so one end of the serial cable must be a D9 male. The other connector on the cable depends upon the RS232 connector used on the computer. The computer may have a D9 or a D25 male connector. Typically computers have a D9 for COM 1 and a D25 for COM 2. However, some newer computers use a D9 for both COM 1 and COM 2. The COM port used on the computer does not matter, however you must ensure that the serial communications program being used has the correct computer COM port selected.

Serial Debug Program

The serial debug program controls the communication from an MC8/B to a computer. The program allows a user to view activity of the unit and to control the unit. The debug program is used extensively to perform audio and video testing of a unit in the audio and video ATE programs. This section will demonstrate an example of using debug to troubleshoot a SHARC SRAM failure.

The MC8/B has four SHARCS on the DSP board organized as pairs: pair 0 and pair 1. Each pair of SHARCS has four SRAMs and one SDRAM. In the case of a SHARC SRAM failure, the debug program can be used to determine which of the four SRAMs is defective. Power on the unit with the RS232 2 port connected to the computer, while the computer is running a terminal program with the correct COM port and protocol enabled. When the unit reports the SHARC SRAM failure and has entered a diagnostic loop with the same error data continuously cycling on the monitor, power off the unit. The data will appear as follows:

“SHARC Failed Test test num: 00000003
test phase: 00000000
sharc address: 02FE000E
sharc byte written: AAAAAAAA
sharc byte read: AAAAAA8A

Sharc Error Code: 0318
sharcpair0_ps2 sram
sharcpair0_ps2 sram test failed, Error code: 0318
DIAG FAIL:ShSRAM_02 E:0318”

Compare the data from the sharc byte written to the sharc byte read. If the failure is a defective SRAM the typical failure mode is to be off by one bit and the byte comparison will determine which IC is at fault. In the above example:

byte written: AAAAAAAA = 1010 1010 1010 1010 1010 1010 1010 1010
byte read: AAAAAA8A = 1010 1010 1010 1010 1010 1010 1000 1010

Since data bit 5 is the one that is not correct, checking the schematics for the SRAM used for pair 0, DSPA and DSPB, that has data bit 5 on it will show which SRAM is associated with the failure. See the chart below for further reference.

SHARC SRAM PIN ASSIGNMENTS:								
	SHARC PAIR 0 **DSPA/PS1 & DSPB/PS2**				**SHARC PAIR 1** **DSPC/PS1 & DSPD/PS2**			
Data Bits:	**U20**	**U19**	**U18**	**U17**	**U12**	**U11**	**U10**	**U9**
D0 = Pin 6	D24	D16	D8	D0	D24	D16	D8	D0
D1 = Pin 7	D25	D17	D9	D1	D25	D17	D9	D1
D2 = Pin 10	D26	D18	D10	D2	D26	D18	D10	D2
D3 = Pin 11	D27	D19	D11	D3	D27	D19	D11	D3
D4 = Pin 22	D28	D20	D12	D4	D28	D20	D12	D4
D5 = Pin 23	D29	D21	D13	D5	D29	D21	D13	D5
D6 = Pin 26	D30	D22	D14	D6	D30	D22	D14	D6
D7 = Pin 27	D31	D23	D15	D7	D31	D23	D15	D7
P/N 350-12456 ICSM,SRAM,128KX8,12NS,3.3V,SOJ								

***Note**:*
The reference designators are from MC8 DSP board revision 1, Lexicon P/N 710-15300.

Error Log

An error log, or ring buffer, containing a log of the last 20 (13h) failures is available. If the error quantity exceeds 20, additional error messages are stored at the first location in the buffer (FIFO). The error log is stored in the non-volatile section of SRAM, and is not able to display all diagnostic errors. For example, SHARC SRAM failures are not reported to the error log. Every failure stored in the error log has six parts:

“#NN E## tXX aYYYYYY

wZZZZZZ rQQQQQQ”

#NN: Error Log Number

The error log location number (in hexadecimal). It goes from 00 to 13. Turning the **encoder knob** clockwise allows one to scroll through all twenty error log locations.

E##: Failure Number

The E stands for error and the hexadecimal after the E indicates test number from the list on the next page.

tXX: Error Code List

NO_ERROR	0x0
ADDR_FAILURE	0x1
DATA_FAILURE	0x2
TIMEOUT_FAILURE	0x3
COUNTER_FAILURE	0x4
NON_VOL_DATA_FAILURE	0x5
OPCODE_FAILURE	0x6
IO_FPGA_ID_NO_MATCH	0x7
DAR_FPGA_ID_NO_MATCH (only for MC12)	0x8
AUDIO_FPGA_ID_NO_MATCH	0x9
ANALOG_FPGA_ID_NO_MATCH (only for MC12)	0xA
VFD_TIME_OUT	0xB
VFD_RAM_ERROR	0xC
TEST_INCOMPLETE	0xD
RS232_WRAP_FAILURE	0xE
SRAM_PREBURNIN_FAILURE	0x13
SRAM_BURN_IN_FAILURE	0x14
EPROM_CHKSUM_FROM_FLASH	0x15
SRAM_FAILURE	0x16
FIFO_ERROR_OVERRUN	0x17
PIC_SN_INVALID	0x18
FLASH_BURN_FAIL	0x19
FLASH_BURN_NO_ROOM_LEFT	0x1A
FLASH_BURN_NOT_FLASH_PART	0x1B
SHARC_TIMEOUT_REBOOT	0x1C
DSP_FPGA_ID_NO_MATCH	0x1D
DEC_FPGA_ID_NO_MATCH	0x1E
DIAG_TEST_NOT_EXIST	0x20
THERMOSTAT_FAILURE	0x21
ERROR_ID_BAD_VALUE	0x40
ERROR_PARAM_SEMA_CREATE	0x60
CS49400_NO_BOOT_START_MESSAGE	0x100
CS49400_NO_BOOT_SUCCESS_MESSAGE	0x101
CS49400_INIT_ERROR	0x102
CS49400_ERR_WRITE_TIMEOUT	0x103
CS49400_ERR_READ_TIMEOUT	0x104
CS49400_INTREQ_TIMEOUT	0x105
CS49400_AUTO_BOOT_FAILURE	0x106
CS49400_ENQ_MSG_FAILURE	0x107

CS49400_DEQ_MSG_FAILURE	0x108
CS49400_FINTREQ_TIMEOUT	0x109
CS49400_NO_APP_START_MESSAGE	0x110
CS49400_AB_SPI_TIMEOUT	0x111
CS49400_C_SPI_TIMEOUT	0x112
CS49400_HOST_BOOT_FAILURE	0x113
CS49400_FLASH_WRITE_TIMEOUT	0x114
CS49400_BAD_FLASH_DATA	0x115
CS49400_BAD_RESP_OPCODE	0x116
CS49400_FLASH_READ_TIMEOUT	0x117
CS49400_MASTER_BOOT_FAILURE	0x118
CS49400_BAD_FLASH_VERSION	0x119
CS49400_ERASED_FLASH	0x11A
CS49400_CHECKSUM_FAIL	0x11B
The sharc error codes use from 0x0300 through 0x03FF	
SHARC_WCLK_FAILURE	0x3F9
SHARC_SRAM_FAILURE	0x3FA
SHARC_SDRAM_FAILURE	0x3FB
SHARC_GPIO_FAILURE	0x3FC
SHARC_RX_TIMEOUT	0x3FD
SHARC_TX_TIMEOUT	0x3FE
SHARC_BAD_OPCODE	0x3FF

The following codes are used to interpret the results from the SHARC GPIO, SRAM, SDRAM, and Word Clock Tests available from the Extended Diagnostic Repair Menu. The Error code is 16-bits with the most significant byte always being 0x03.

The least significant byte is broken into bits as shown:
”(MSBit) B7 B6 B5 B4 B3 B2 B1 B 0 (LSBit)”

- B7 - Semaphore indicator, 1 failed, 0, passed.
- B6 - GPIO LED failure, 1 indicates that neither LED lit up from the test.
- B5 – Read Back Reg Fail, 1 indicates the Readback register failed.
- B4 - Test Fail, 1 indicates the test failed, 0 success.
- B3 - SHARC Test Completed. 1 indicates that the sharc was able to finish executing the test.
- B2 - READ Timeout, 1 means that Z180 could not read back from the SHARC. 1 indicated timeout.
- B1 - WRITE Timeout, 1 means there was a timeout.

- B0 - SHARC write timeout id 0 is for PS1, 1 is for PS2.
- If there is a WRITE TIMEOUT, then check B0 to see which SHARC in the pair caused the fault.
- B3 shows if the SHARC was able to run the code, and determine whether there was success or failure. Success or failure can be determined by either the GPIO LEDs, green success, red failure, or by the return code in the register readback, 0xAA for success and 0x55 for failure.
- If B4 is 0, then make sure that B3 is 1 before deciding whether the SHARC test passed.
- If the GPIO LED failure bit indicates a failure, then check the circuitry surrounding the LED. An LED failure occurs when the number of LEDs lit is NOT 1. If 2 are lit, then there is probably a short between them. If 0 are lit, then parts may be missing, or a short exists.
- Bits B2, B1 and B0 are read together. If a time out occurs then B2 or B1 will indicate what operation caused the fault. B0 will indicate which processor failed, Processor A or B.
- Bit B3 is used to indicate whether the SHARC was able to run the code. If this bit is zero, the code was not able to run, a 1 indicates the SHARC was able to run.
- Bit B4 indicates whether the test passed or failed. This bit is only valid if B3 is a 1.
- Bit B5 indicates that the read back register failed. There is a fault in the read back register circuitry if this bit is a 1.
- Bit B6 indicates whether the circuitry around the SHARC LEDs failed. A 1 indicates a failure.

When the SHARC passes these tests, it will return a value of 0x0300.

aYYYYYY: Failing address location

The address (in hexadecimal) where the failure occurred.

wZZ: Value Written

The target value (in hexadecimal) that was written to the address where the failure occurred.

rQQ: Value Read

The actual value (in hexadecimal) that was read from the address where the failure occurred.

The error log is available as a menu item in the extended diagnostics under Repair Tests. In addition, the error log can be viewed on an external PC or terminal via the D9 connector labeled RS232 2 on the rear panel of the MC8/B. The error log is sent to RS232 2 when the VIEW ERRORLOG selection is made.

Power On Diagnostics

As described earlier, there are two power-on modes in the MC8/B. Power on via the rear panel power switch and by coming out of standby mode. Power-on diagnostics are executed every time the rear panel power switch is switched on. Diagnostics are not run when the unit is brought out of Standby mode.

Power-on diagnostics take approximately forty seconds to complete. The power-on diagnostics are intended to verify basic hardware functionality of an MC8/B. Additional diagnostic tests are available for manufacturing and customer service to completely test the hardware, and for debugging failures.

Initially, an attempt is made to illuminate the VFD and front panel LEDs for approximately five seconds. However during the first six tests the VFD will not be considered functional due to it not being tested. During these tests, Trap Op Code, EPROM, FLASH Checksum, Z80 SRAM, program FPGAs, and VFD RAM, the unit will attempt to use the STANDBY LED to indicate if a failure occurs. As soon as these are completed the VFD will display:
“DIAGNOSTIC TESTS

… …”

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This communicates that the unit is still functioning. The audio outputs (digital and analog) will be muted during this sequence.

The following sections list the test explanations. The front panel display is shown only for the first test that can use the VFD. The reference designators used are for the MC8 Revision 3 Main Board 710-15250 used on BOM 023-15428, and revision 0 memory board used on BOM 023-15429. The schematic for the main board is 060-15259, and the memory board is schematic 060-15299.

Trap Opcode

The Trap Opcode error occurs if during the initial boot sequence an undefined Opcode is fetched. The INT/TRAP Control register can be used to determine the starting address of the undefined instruction. If the trap error occurs an attempt will be made to blink the STANDBY LED using a rate of a single blink per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

EPROM Checksum Test

The EPROM Checksum test verifies the 2 Meg 27C020 EPROM, U3 on the Memory Board, has the correct program by adding up all the values in each bank of the EPROM. The test verifies the separate banks and the bank switching of the MC8/B. The checksum of each bank is reported to the Serial Debug Port. The test verifies that the calculated checksum in each bank matches the checksum value stored in the EPROM. If an error occurs an attempt will be made to blink the STANDBY LED using a rate of two blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

Z180 SRAM Test

The Z180 SRAM test performs non-destructive testing on the 256k SRAM, U90 on the Main board, on page 2 of the main board schematics. The non-destructive test first saves the data in the location being tested. Then that location is tested by writing and reading patterns 0x00, 0xFF, 0x55, 0xAA, 0x01, 0x02, 0x04, 0x08, 0x10, 0x20, 0x40, and 0x80. The original data is then returned to the SRAM and the next location tested. Once each location in the SRAM is verified, a counting-memory check is done throughout the SRAM to test buss integrity. First, each byte in a special 32-byte section is written with a count. Then,

starting from the beginning of the block, and incrementing through it, the count is verified to be correct. If so, this area will be used to store the contents of the rest of SRAM as it under goes the count check in 32-byte blocks. If an error occurs, an attempt will be made to blink the STANDBY LED using a rate of three blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging. In order for the test to pass the Z180 and the CPLD, U84 and U83 respectively on the main board and page 1 of the schematics, and associated support circuitry must be functioning.

Flash Checksum Test

The Flash checksum test verifies the data in the 16 Meg flash memory, either U1 or U2 on the memory board. For all banks the checksum test adds up all the data in each bank except for the bank number and stored checksum locations (stored in the last three locations of each bank). The added value is then verified against stored values. If an error occurs, an attempt will be made to blink the STANDBY LED using a rate of four blinks per several seconds and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

DISPLAY FOR THE REMAINING TESTS

If any of the following tests fail the VFD display and LED matrix will display the test and error fault, if one occurs, as previously discussed. The VFD will display the test number and the error code. In the event that the VFD is not operable, the same information will be written to the LED matrix. The test number will be read out as in the top row. The error number can be read out in the second row (Most Significant Byte) and third row (Least Significant Byte).

Vacuum Fluorescent Display (VFD) Test

The VFD performs a busy test and a memory test. The busy test sends information to the VFD and verifies that the VFD asserts then de-asserts its busy status. The VFD memory test consists of writing 55h, AAh, a walking 1 and finally a 0 to the character generator memory and display memory space of the VFD and reading them back. After the MC8/B has passed the VFD Test, for the rest of the power on diagnostics, the VFD displays:
”DIAGNOSTIC TESTS
… …”

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This keeps a user informed as to the functioning of a MC8/B.

If a failure occurs, the test will attempt to write an entry into the error log and enter a loop to exercise signal lines to aid in debugging. The error log is stored in the non-volatile section of the SRAM so that it is not destroyed during the power on diagnostics. A single error log entry is made each time the MC8/B is powered up, a diagnostic test is executed, and a failure encountered.

I/O FPGA Test

The I/O FPGA test loads and verifies the programming of the XCS05-VQ100, U67 on the main board, on page 2 of the schematics. The I/O FPGA is used to program the other DAR FPGA, the Audio FPGA, and the Analog FPGA. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

DSP FPGA Test

The DSP FPGA test loads and verifies the programming of the XCS05-VQ100, U7 on the DSP board revision 1 and page 8 of the schematics. The Audio FPGA must be functioning since it is used to program the DSP FPGA. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Decoder FPGA Test

The Decoder FPGA test loads and verifies the programming of the XCS05XL-VQ100, U4 on the decoder board and page 2 of the schematics. The Audio FPGA must be functioning since it is used to program the Decoder FPGA. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Crystal 49400 Test

This test verifies that the Crystal 49400, U2 on the decoder board and page 3 of the schematics, can communicate with the Host Z180 processor through the Audio FPGA. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

SHARC SDRAM Test

This test verifies that the SDRAM for each SHARC that has this test enabled on the DSP board is operational and can be written to and read from. The SDRAM test is run using SHARC Pair 0 Processor A and the SDRAM is U14 on the DSP board and page 4 of the schematics. The SDRAM test is also run using SHARC Pair 1 Processor C, which is U4 on the DSP board and page 7 of the schematics. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

The test writes the test patterns of 0x55555555, 0xAAAAAAAA, a walking 1 and 0x00000000 are written to each location and read back. Once each location is verified, a counting test is applied to verify the address buss.

SHARC SRAM Test

This test verifies that the SRAM for each SHARC that has this test enabled on the DSP board is operational and can be written to and read from. The SRAM test is run using SHARC Pair 0 Processor B, and the SRAMs are U17-U20 on the DSP board and page 4 of the schematics. The SRAM test is also run using SHARC Pair 1 Processor D and the SRAMs are U9-U12 on the DSP board and page 7 of the schematics. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

The test writes the test patterns of 0x55555555, 0xAAAAAAAA, a walking 1 and 0x00000000 are written to each location and read back. Once each location is verified, a counting test is applied to verify the address buss.

Power On Diagnostics Completed

After the power-on diagnostics are completed the VFD will display the appropriate power up message:

“MANUFACTURER MODEL VX.XX
(c) 200X OPTIONS”

At this point the operating system takes over the functioning of the MC8/B.

EXTENDED DIAGNOSTIC TESTS

As described earlier, the extended diagnostic tests are accessible by pressing and holding the MAIN VCR and ZONE 2 VCR front panel buttons when powering on a MC8/B. The audio outputs (analog and digital) are muted. When the VFD displays “LEXICON,” the front panel buttons can be released. After the model banner is briefly displayed on the VFD, the display will indicate:

“DIAGS MENU
FUNCTIONAL TESTS”

The extended diagnostics can also be entered via the serial debug port by first entering the debug program. Type “debug” when connected to the RS232 2 serial port to access the debug program. The debug program is case sensitive. Once in debug, type “x 2e” and the unit will go into extended diagnostics. In addition the extended diagnostics can be entered through the RS232 2 serial port by sending “ed” which stands for extended diagnostics, to the unit via the serial debug port during the first ten seconds after powering on the unit.

After extended diagnostics are entered, use the front panel encoder, Mode ▲ and Mode ▼ buttons to navigate through the diagnostics. The front panel encoder is rotated to display the desired tests. Press the Mode ▼ button to move down through the menu selections and to execute the desired diagnostic test. Use the Mode ▲ button to back up through the menu selections similar to an escape (ESC) button on a computer keyboard.

Types of Tests

The extended diagnostic tests fall into two categories: functional and repair. The functional diagnostic tests are required to functionally verify an MC8/B and are performed on every unit. The repair, or troubleshooting, category is for troubleshooting defective units. The repair tests are used only if there is a failure. The repair tests can be used to help isolate the source of failures so that units can be cost effectively fixed.

Two groups of functional tests are executed on every MC8/B: Loop Tests and the Functional Test Suite. These tests comprise the automated set of diagnostic tests used to verify functional operation of every unit. All of the diagnostic tests in the loop tests and in the functional test suite are run in sequence. If there is a failure the failing test will loop to allow the electrical signals to be active for troubleshooting. The operator can optionally continue the diagnostic tests to see what other diagnostic tests might be failing.

User Interface

The user interface consists of a set of menus. The top menu is the "DIAGS MENU" and is shown in the top line of the VFD display. To view the available menu items turn the encoder knob in either direction and the menu choices will appear in the second row. The available choices are Functional Tests, Repair Tests, Loop Tests, Audio I/O Tests, Video I/O Tests, and Normal Operation. When the desired menu item is shown, press the Mode ▼ button. This selects the menu item. If the item is another menu, the menu's

title now appears in the top line of the VFD and its menu items are in the second row. If a test is selected, the test name will appear in the top line and the results or information to run the test will be on the second row. Once a test is finished, or to get out of a menu press the Mode ▲ button. Pressing and holding the Mode ▲ button returns you to the top-level diagnostic menu.

There are groups of diagnostic tests in which if a test passes, the diagnostics automatically execute the next test. Group tests are the Power-On Diagnostics, in the Manufacturing suite, the Pre Burn-In test, and the Burn-In Loop. For the Burn-In Loop, upon successful completion of the group tests, the VFD will briefly display either "Pass" or "Fail", and continuously loops until power is removed from the unit.

If a test fails, the VFD and front panel LEDs, will attempt to indicate the failed test. The test will attempt to loop to keep the signal lines active for debugging purposes. If an individual test is selected, it will continuously run and report if it passes every time it successfully completes the test. In addition, test progress and failure information is available via the serial debug port. Specific failure information will depend on the test being executed.

REPAIR DIAGNOSTICS SUITE

The Repair Diagnostics suite allows you to individually execute every diagnostic test on a unit. The Functional suite uses the same tests as the Repair Diagnostic suite, but automates how the tests are run.

The following tests are available in the Repair Diagnostics:

- Z180 EPROM checksum
- Z180 FLASH checksum
- Z180 SRAM
- I/O FPGA Verify
- RS232 Wrap Test
- SHARC Tests

    Sharc GPIO (x12)
        PAIR 0 PROC A
        PAIR 0 PROC B
        PAIR 1 PROC A
        PAIR 1 PROC B
    Sharc SRAM (x12)
        PAIR 0 PROC A
        PAIR 0 PROC B
        PAIR 1 PROC A
        PAIR 1 PROC B
    Sharc SDRAM (x12)
        PAIR 0 PROC A
        PAIR 0 PROC B
        PAIR 1 PROC A
        PAIR 1 PROC B
    Sharc WCLK(x12)
        SEL 44 WORD CLK
        SEL 48 WORD CLK
        SEL 88 WORD CLK
        SEL 96 WORD CLK
        SEL 44-48 PLL WCLK

- SEL 88-96 PLL WCLK
- SEL DRCVR WCLK
- PAIR 0 PROC A
- PAIR 0 PROC B
- PAIR 1 PROC A
- PAIR 1 PROC B

Sharc Boot (x2)

- PAIR 0
- PAIR 1

DSP FPGA Verify
CS49400 Boot Test

- FPGA ID Test
- Boot Test
- Show Flash Version
- Flash Checksum Test
- Load Flash

IR Remote
VFD Memory Test
VFD CHAR Test
VFD BLOCK Test
OSD CHAR Test
SWITCH Test
LED Test
ENCODER Test
VIEW ERRORLOG
Clear NON-VOL SRAM
Set Triggers (x3)

- TRIGGER 0
- TRIGGER 1

Expand Output MUTE
MIC DSP CONN Test
Set FAN Test
Show Serial NUM
PIC SN Validity
Flash Burn Test
Thermostat Test
Set Constant Cycle
Normal Operation

The extended diagnostic tests that are the same as in the power-on tests are not described here.

FUNCTIONAL DIAGNOSTIC SUITE

The manufacturing suite is available from the top level DIAGS MENU and the FUNCTIONAL TESTS item is selected.

1. When you select the menu item, the VFD will display:

   "FUNCTIONAL TESTS
   START ALL TESTS"

   There is only one menu item in this menu, and selecting it will start the sweep through the whole repair suite. As long as there are no errors, the test will continue until the tests requiring an operator response are encountered. If there is a failure, the offending test will cycle and the error code will be displayed on the second line. For example, if the DEC FPGA verify fails the VFD will display:

   "DIAGNOSTIC TESTS
   DEC FPGA E:001E"

2. To continue, hit the **MODE ▲** button.

   Some tests require you to help with the test by pressing the **MODE ▲** key, or by turning the **encoder** to iterate through the test.

3. Upon completion of all of the tests, the second row of the VFD displays "Pass" or "Errors."

RS232 Wrap Test

This test verifies the RS232 ports are working by comparing the transmitted signal (at pin 2s of J5) to the received signal (at pin 3s of J5). If the signals are the same, the test passed. In order to test this circuit, (2) RS232 Wraparound plugs are needed and must be installed at the female D9 connectors (J4 & 5) on the rear panel of the MC8/B labeled "RS232." Once these plugs are installed, the test can be executed.

1. When you select the test, the display will read:

   "EXTENDED DIAGNOSTICS
   RS232 Test"

   All buttons except for the **Mode ▼** will be inactive. The **encoder knob** is active to select another test.

2. Press the **Mode ▼** button to execute the test. The display will read the following if both ports pass:

   "SERIAL PORT A PASSED
   SERIAL PORT B PASSED"

   If Serial Port A Failed, the display will read:

   "SERIAL PORT A Failed
   SERIAL PORT B PASSED"

   If Serial Port B Failed, the display will read:

   "SERIAL PORT A PASSED
   SERIAL PORT B Failed"

   If both Serial Ports Failed, the display will read:

   "SERIAL PORT A Failed
   SERIAL PORT B Failed"

   To troubleshoot this type of failure, use the front panel **Mode ▼** button. Each time the button is pressed, a message is sent out the RS232 port at pin2 of J4. This will activate the COM0_TX0 signal coming from the Z180 pin 48. In the situation where the test passes, the COM0_RX signal is present

at Z180 pin 49 as long as the wraparound plug is connected. Another way to test this circuit is to verify the IR Receiver (green) LED lights briefly when the button is pressed. This approach can be helpful when troubleshooting intermittent failures.

***Note**:*
If the unit is attached to a debugging PC, then serial port A will fail. However, if the PC's terminal software is showing results and the user is able to type in commands or run debug scripts, then the port is working.

Thermostat Test

The thermostat test verifies the temperature sensor installed at U66 on the main board. To verify the IC's functionality, a shorting jumper is installed at W1. This shorting jumper changes the resistance presented at pin 2 of the temperature sensor. The temperature sensor sets the temperature it detects via a resistor divider network. Grounding pin 2 will cause the diagnostic test to verify the TEMP signal lines have changed state.

1. Upon entering the test the VFD will indicate:

   "THERMOSTAT TEST
   Insert Jumpers"

2. If the test passed when the **MODE ▾** button is pressed the VFD will indicate:

   "THERMOSTAT TEST
   Test: PASSED"

   The diagnostic test will then prompt for the jumper to be removed.

   "THERMOSTAT TEST
   Remove: jumpers"

   If the jumpers are not removed the test will prompt a second time to have the jumpers removed.

   "THERMOSTAT TEST
   Jumpers not removed!"

Fan Test

The fan test verifies operation of the fan.

1. When you select the test, the VFD will indicate:

   "SET FAN
   FAN: OFF"

2. Rotate the **encoder knob** clockwise and the VFD will indicate:

   "SET FAN
   FAN: ON"

   The fan will be spinning.

3. Rotate the **encoder knob** counter-clockwise and the VFD will indicate:

   "SET FAN
   FAN: OFF"

   The fan will stop spinning.

IR Remote

This test verifies the functionality of the IR Remote by pressing on the remote and verifying that the VFD displays which IR remote button was pressed. The VFD displays (in hexadecimal) the code received when a remote key is pressed. The hex display on the VFD remains unchanged until another remote key is pressed. While the remote key is being pressed the IR acknowledge LED will flash and the VFD displays the message "IR", (without the quotes), next to the hex value. When you have successfully exited the test the VFD will display an arrow on the left side pointing to the word REMOTE.

1. When you select the test, the display will read:

   “IR REMOTE
   Remote Test:”

   All buttons except for **Mode** ▼ will be inactive.

2. When you hold down a remote button, such as the **DVD 1** button, the display will read:

   “IR REMOTE
   Remote Test: 20IR”

   The 20 is the hex code for the DVD 1 button, IR is displayed to indicate the remote is currently transmitting a signal, and the amber IR acknowledge LED will be flashing. As different buttons are held down, the hex code will change indicating which is being pressed.

VFD Character Test

The combination of the Character Test and the Block Test verifies that all display segments are functioning. The Character Test places the same character on all VFD segments. The ENCODER knob is then used to change the character. The test has sufficient variation of characters to verify complete functionality of the VFD. All characters present in the VFD can be observed.

1. When you select the test, the VFD will display all “As” as shown below:

   “AAAAAAAAAAAAAAAAAAA
   AAAAAAAAAAAAAAAAAAA”

2. Rotate the **encoder knob** to view other characters. To exit the test, press the **Mode** ▲ button.

VFD Block Test

***Note**:*
*When rotating the **encoder knob** sometimes pixels on the VFD will randomly flicker very briefly. This is normal operation.*

The Block Test illuminates all pixels on a single segment of the VFD. The **encoder knob** is then used to move the block to each segment.

Press the **EFFECT DOWN** button to execute the test. The display will read:

“■”

Rotate the **encoder knob** clockwise to move the block through all VFD locations. At the end of the line, the block will wrap to the next line. In the case of second line the block will return to the starting point on the first line.

Switch Test

This test will verify all twenty-two front panel switches are working. Each button on the front panel is pressed and the VFD will indicate which front panel button has been pressed.

Example: Switch Test: MODE_DN in the second line on the VFD.

If the button has an LED associated with it, the LED will illuminate. When all switches have been tested, the bottom half of the display will indicate completion.

Encoder Test

The Encoder Test verifies the operation of the encoder knob including direction and the twenty-four positions. It is designed so that if there was a bad position on the encoder knob, the display will never indicate a "Passed" message. This is achieved by having the accumulator value reset to 0 if a switch position was bad or if the encoder was turned in the opposite direction during the test. Therefore, the accumulator will never see the expected value of 24 so the program would not be able to perform the next task (i.e. instruct the user to perform the counter-clockwise test or display "Passed"). When the encoder is being tested, the bottom right half of the display will indicate the direction and position value. The test requires the clockwise direction to be tested first.

1. When you turn the **encoder knob** clockwise, the display will read:

   “EXTENDED DIAGNOSTICS
   Encoder Test CW 05”

   In this example, the **encoder knob** was turned five positions clockwise.

2. After the **encoder knob** is turned one (1) revolution clockwise (covering all twenty-four positions) the display will read:

   “EXTENDED DIAGNOSTICS
   Encoder Test CCW 24”

   The bottom half of the display (CCW 24) indicates the counter-clockwise test is ready to be executed.

3. After you turn the **encoder knob** one complete revolution counter-clockwise (covering all positions), the display will read:

   “ENCODER TEST
   Encoder test passed”

LED Test

The LED test illuminates each LED by turning the **encoder knob** clockwise or counter-clockwise. As the **encoder knob** is turned each individual LED is illuminated.

Expand Output MUTE Test

The Expand output MUTE test verifies that the MUTE signal going to the XLR board is functioning.

1. When you select the test, the VFD display will indicate:

   "EXPAND OUTPUT MUTE

   EXPOUT: Low"

   On the main board the red LED D23 will be lit when the VFD indicates that the EXPOUT signal is low.

2. Rotate the **encoder knob** clockwise and the VFD will indicate:

   "EXPAND OUTPUT MUTE

   EXPOUT: High"

   And the red LED at D23 will be off. If the unit being tested is a MC-8 Balanced, the relay on the XLR board can also be heard. Turn the **encoder knob** counter-clockwise to set the expand-and mute signal low.

Trigger Test

This test will verify the trigger circuits of the MC-8. For this test you will need the MC-8 remote control and a Digital Multimeter (DMM).

Test:

1. Power on the MC-8.
2. Turn on the DMM and set it to read DC voltage for a 12V level.
3. Using the remote control Menu ▸ arrow, select SETUP form the Main Menu.
4. Scroll down through the SETUP menu and select TRIGGERS.
5. Scroll to DVD1 and change the trigger from OFF to ON.
6. Ress the remote control MAIN button, then press the remote control DVD1 button to select DVD1 as the input for the Main Zone.
7. On the MC-8 rear panel, locate the Trigger Outputs block.
8. Connect the DMM's red probe to positive (+) and connect the black probe to negative (-). Measure the PWR +/- and the #1 +/- trigger outputs for 12 volts DC.

PIC Software ID Test

The functional diagnostics will now automatically perform the PIC S/N test, which verifies that the software ID programmed into the PIC microcontroller is within the range allowed per the Lexicon specification sheet.

REPAIR DIAGNOSTICS SUITE

View Error Log

This is not a test but it enables you to view the contents of the error log. Turning the **encoder knob** allows you to view the error log contents.

Clear Non-Volatile RAM

This is not a test, but allows you to clear out the error log contents and other areas of RAM that are not cleared on a power up.

1. When you select this menu item, the display will show:

   "CLEAR NON-VOL SRAM

   Confirm - Press MUTE"

2. When **MUTE** is pressed, the second line will display:

   Initializing RAM for a second, then it will display:

   "TEST COMPLETED"

LOOP TEST SUITE

The Loop, (burn-in) suite is available from the top level DIAGS MENU when the LOOP TESTS item is selected.

1. When you select LOOP TESTS, the VFD will display:

   "LOOP TESTS
   NON_VOL RAM SETUP"

   The NON_VOL RAM setup initializes the non-volatile section of the SRAM with a byte pattern that is verified by the loop tests. As the unit is in burn-in, this byte is continuously verified ensuring that the register section of the SRAM continues to hold data. This will also set a flag for programming the decoder and video flash memories at the beginning of the burn-in loop the first time the test is run.

2. Rotating the **encoder knob** will display the following on the VFD:

   "START ALL TESTS"

   When the Start All Tests menu option is selected, the Loop tests are run continuously. The first time the burn-in loop is run the decoder flash and the video flash will be programmed. They will each take about 3.5 minutes to complete. This flash programming is only performed one time. All subsequent looping of the burn-in loop will not program the flash.

These are the tests available in the Loop Test Suite:

- Z180 Burn-In SRAM
- Z180 EPROM checksum
- Z180 FLASH checksum
- VFD Memory

- I/O FPGA Verify ID
- DSP FPGA Verify ID
- Decoder FPGA
- Crystal 49400 Boot
- Sharc Internal GPIO (x4)
- Sharc SRAM (x4)
- Sharc SDRAM (x4)
- Sharc Boot (x2)
- Trigger 0 ON
- Trigger 1 ON
- Trigger 0 OFF
- Trigger 1 OFF

There is only one item in this menu and selecting it will start the sweep through the whole suite of loop tests. As long as there are no errors the test will continue to run. If there is a failure, the entire bottom row of eight LEDs on the front panel will light. These are the TV, CD, TUNER, and AUX LEDs for the Main and Zone2 sections. Depending upon the failure, the failing test will cycle and the error code will be displayed on the second line of the VFD. For example, if the Decoder FPGA verify fails the VFD will indicate:

DEC FPGA TEST
Fail: E 001E

To continue, press the **MODE** ▲ switch.

Upon completion of all of the tests, the second row of the VFD will briefly indicate “Pass” or “Errors”.

Loop SRAM Test

The Burn-In SRAM Test reads a bit-pattern from a known location by the NON_VOL RAM SETUP.

AUDIO I/O TESTS

The Audio I/O tests contain the following tests:

- Audio Input 1 Test
- Audio Input 2 Test
- Audio Input 3 Test
- Audio Input 4 Test
- Audio Input 5 Test
- Audio Input 6 Test
- Audio Input 7 Test
- Audio Input 8 Test

- SPDIF Input CX1 Test
- SPDIF Input CX2 Test
- SPDIF Input CX3 Test
- SPDIF Input CX4 Test
- SPDIF Input OP1 Test
- SPDIF Input OP2 Test
- SPDIF Input OP3 Test
- SPDIF Input OP4 Test

These tests put the unit into a state to pass audio through the path that is contained in the test name for troubleshooting. For instance the Audio Input 1 Test would pass analog audio from analog input 1 to all the outputs.

VIDEO I/O TESTS

The Video I/O tests contain the following tests:

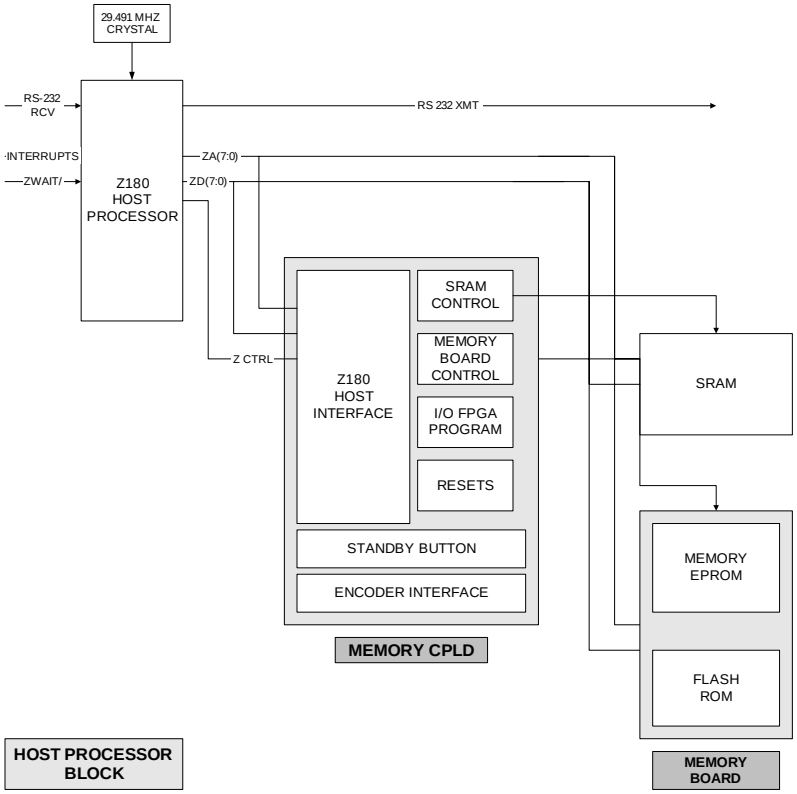
- INIT INT SYNC
- INIT EXT SYNC
- Select PAL
- Select SECAM
- Load Font
- Color Bars
- Show CHARS

The video I/O tests initialize the video circuitry to put the unit into a known state for troubleshooting. The menu items select a few of the basic setups that can be used for troubleshooting. These selections will instruct the On Screen Display, OSD, IC in the unit to output a video signal that can be used to verify the video circuit from the OSD to the monitor outputs of the unit.

CHAPTER 6 – THEORY OF OPERATION

Main Board Z180 Host Processor

The Z180 is responsible for all systems control in the unit. It runs off the 29.491mHz crystal oscillator. It is reset by the main **PWR_RST/** signal. ZCLK is a buffered synchronous clock output that is used to synchronize signals in the Memory CPLD and the I/O FPGA.



Memory CPLD

The Memory CPLD is programmed at the factory like an EPROM. It can be programmed before or after it is soldered to the PC board. It provides the following functionality:

- Host data, address and control interface – provides all memory space address decoding, plus a small section of I/O space that is occupied by the Memory CPLD internal control and status registers
- SRAM read/write signals and bank address bit
- Flash ROM and EPROM control signals and bank address bits, **RA(22:15)**
- The I/O FPGA programming bits
- Reset lines under host control to the analog circuitry, I/O FPGA, Video Board, and Front Panel Board
- The Standby LED
- The Standby button
- The Front Panel Encoder interface.

Host Processor Memory

There are three devices located in the Z180's memory space; the SRAM, which is on the Main Board, and the FLASH ROM and EPROM, which are located on the Memory Board. The 32kx8, 70ns SRAM is powered by the battery backup, **BAT_VCC**, so that user and factory default settings are preserved when the unit is powered down.

The Z180 boots from the 256kx8 70ns EPROM at power up. Once the EPROM, SRAM and FLASH diagnostics have passed the Z180 sets a bit in the Memory CPLD that allows the Z180 to run out of the FLASH ROM. The 2Mx8 FLASH ROM is programmable from the RS-232 serial port.

Host Processor I/O

All peripheral devices and boards live in the Z180 I/O address space. The I/O FPGA handles all address decoding. Due to the size of the Main Board, the Z180 data bus is buffered through two 74VHCT245s, creating the **IODX** and **IODY** data buses. All data and address buses going to other boards are also buffered.

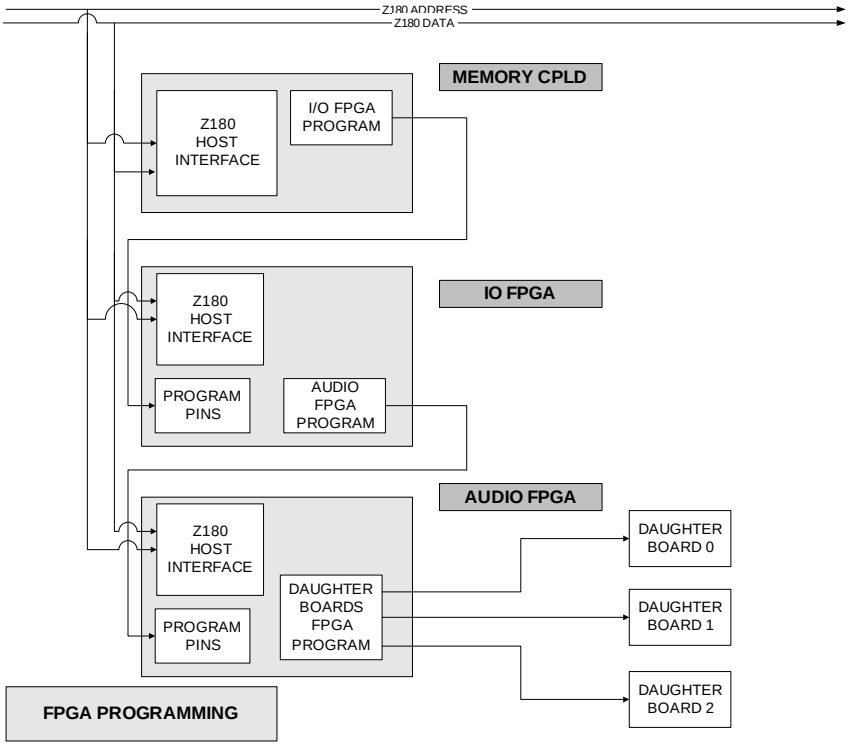
RS-232 Serial Interface

The 29.491mHz crystal oscillator is divided down to provide the 19.2K Serial Baud Rate of the MC-8. The TX0, RX0, TX1 and RX1 ports on the Z180 are connected to the Max202E Transceiver that drives the two female DB9 connectors RS-232 1 and 2.

FPGAs

Host Programming of FPGAs

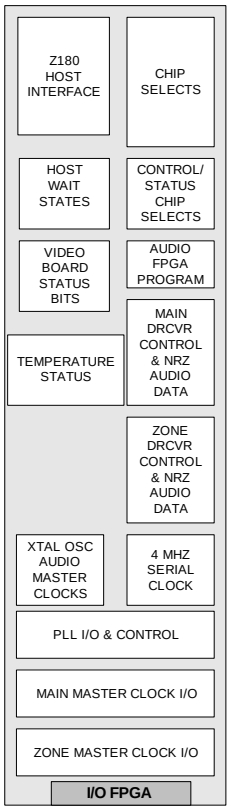
All FPGAs are programmed by the Host processor as part of the boot process when the unit is powered on from the rear panel. The I/O FPGA is programmed by the host through the Memory CPLD. The Audio FPGA is programmed by the host through the I/O FPGA. Any FPGAs residing on daughter boards are programmed through the Audio FPGA. It is important to understand that until the FPGAs have been programmed, most of the unit, including the front panel and on screen display are in reset. There are LEDs that light to indicate when the programming for each FPGA is complete.



I/O FPGA

The I/O FPGA has a byte wide data path for the host interface. It provides the following functions:

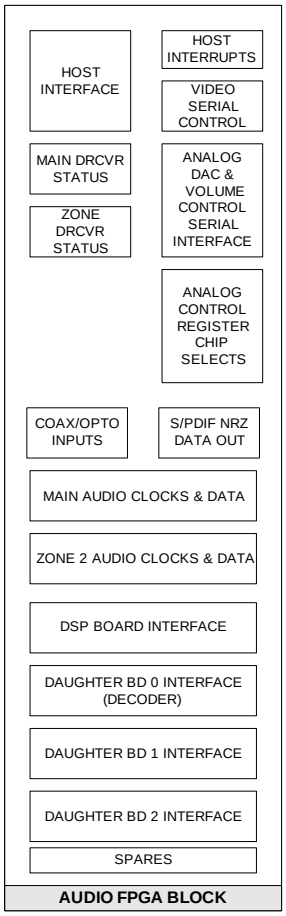
- Handles the entire I/O space memory map for the system
- Generates the chip selects for all peripheral devices that the host communicates with over the I/O data bus
- Automatically generates wait states to the Host for devices that require longer access times.
- Outputs the bits that are used to program the Audio FPGA
- Receives Video Board status
- Receives temperature sensor status
- Generates 4mHz clock used for serial control interfaces
- Allows the host to choose between the crystal oscillators for analog audio, the master clock output of the Digital Receivers or the output of the Phase Lock Loop (PLL) as the master clock source for each zone.
- Digital control signals for the PLL
- Control bits and sample-rate detection clocks to the Main and Zone Digital Receivers.



Audio FPGA

The Audio FPGA is the central audio routing block for the system. It has a byte-wide data path to the host and seven host address lines. It performs the following functions:

- Generates word and bit clocks for each zone from the master clocks and distributes them to all audio devices and interfaces on the main board
- Allows the host to select which digital audio connector is connected to the Main and Zone Digital Receivers
- Receives status bits from the Main and Zone Digital Receivers
- Host Serial Control Interface to the to the Video Board and On Screen Display. Consists of the chip select, serial clock and data. The FPGA converts the host parallel data to a serial data stream
- Serial control of the Main and Zone DACs and Volume Controls
- The 1mHz clock signal used by the 16C54 PIC IR Receiver
- Routes all I2S audio data in the system
- Packs and unpacks I2S audio into octal streams for the Sharc DSPs
- Provides interrupts to the Z180 Host processor
- Provides twelve programmable tie lines each to the DSP board connector and the three daughter board connectors.



HOST INTERFACE TO OTHER BOARDS

Front Panel, IR/Encoder, and VFD

The interface to all of the front panel boards (with the exception of the standby board) is a single ribbon connector. All signals are connected to the Switch/LED Board. It then passes signals as required to the IR/Encoder Board and the VF Display.

The signals used by the Switch LED Board are as follows:

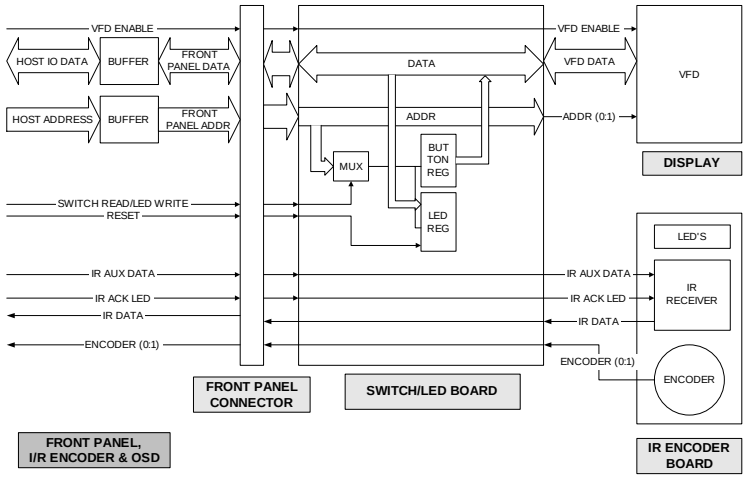
- FP_RST – this prevents the LEDs from lighting when the unit is first powered up, until the host is initialized
- SWRD_LEDWR/ - when this signal is high, the MUX generates the enable for reading the Switch Buffer. When it is low, it generates write strobes to the LED Registers and the Switch Column register. In order to read the switches, the host must first select a column
- Front Panel data – bi-directional
- Front Panel address – used by the MUX.

Signals used by the VF Display are as follows:

- VFD_EN_BUF – chip select to the display
- Data – byte-wide
- Address – two address bits. Address determines whether an access is a read or a write.

Signals used by the IR/Encoder Board are as follows:

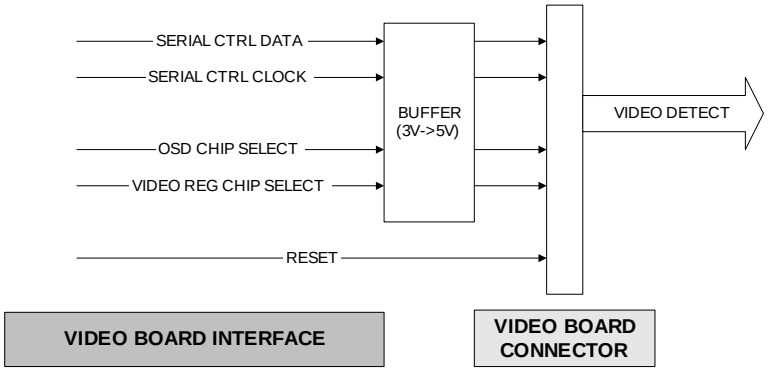
- IR auxiliary data from the rear panel connector. This is optically coupled with the incoming IR signal at the IR receiver
- The IR acknowledge LED bit. This comes from the PIC and is used to indicate that the unit is detecting an infrared signal
- System_On and Overload LED bits
- Encoder 0:1 – these are the output of the front panel encoder knob. They are read and interpreted on the main board.



Video Board & OSD

The control interface to the Video Board consists of:

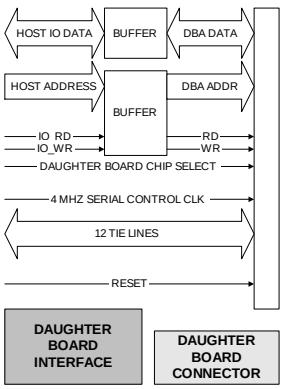
- Serial control data
- The serial control bit clock
- OSD chip select – enables the serial control port of the On Screen Display chip
- Video Register chip select – enables the serial to parallel registers that generate the control bits used on the video board
- The video reset line.



DSP and Daughter Board Connectors

The DSP and daughter board connectors have the following interface:

- Host I/O data bus
- Host I/O address bus
- Host I/O control – RD, WR and CS
- Reset
- 4 MHz clock used on the analog board to derive serial control clocks
- 12 programmable tie lines to the Audio FPGA which can be used as needed for audio clocks and data or control
- 1 programmable tie line to the I/O FPGA.



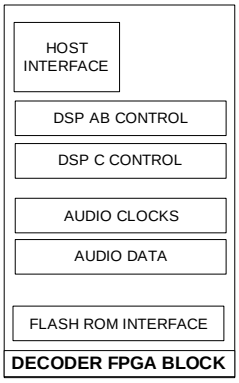
DECODER BOARD

The Decoder board is installed in the Daughter Board 0 slot.

Decoder FPGA

The Decoder FPGA has a byte wide data path for the host interface with 5 bits of addressing. It provides the following functions:

- Provides ABOOT/IRQ and HINBUSY/ lines for control of the Cirrus 49400
- Converts Host parallel data for serial control of the 49400 DSP AB and C
- Uses the MCKI daughter board audio clock inputs DB_MCKI and DB_FSI to create the input and output frame sync and SCLKs required by the 49400 audio interface. This includes running the input and output sides of the CS49400 at different rates for DTS 96/24 decoding
- Uses the Decoder GPIO pins to enable the correct Decoder
- Flash write signals and addresses
- Routes audio data to and from the CS 49400. The input is a single I2S 2-channel PCM data line. The output of the chip consists of four I2S 2-channel PCM data lines.



CIRRUS CS49400 DSP Audio Decoder

The CIRRUS DSP is responsible for detecting and decoding all compressed audio data formats, Dolby AC-3 and DTS. It is a 2.5-Volt part. Its processor clock is a 12.288 MHz crystal oscillator. The internal speed at which the chip runs is selected by DEC_CLK_SEL. The chip actually consists of two linked processors, which are referred to as DSP AB and DSP C. In the following section, (x) refers to AB or C.

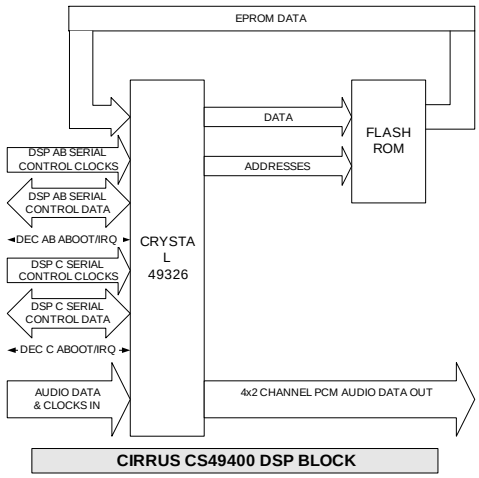
To boot the chip, the Host processor sets the DEC_(x)_ABOOT/IRQ pin low and sets the ECODER_RST/ pin high. The chip then boots from the external Flash Rom. Processor C boots first, followed by processor AB. The host, through the CS49400, can program the Flash ROM. During run time, the host communicates with the Crystal Decoder through a serial control interface that consists of the following signals:

- DEC_(x)_SCDIN – host serial control data generated in the DAR FPGA
- DEC_(x) SCDOUT – CS49400 Decoder status data output to the host
- DEC_(x)_SCCLK – serial data bit clock
- DEC_(x)_CS/ - serial port chip select
- DEC_(x)_ABOOT/IRQ/ - CS49400 interrupt to the host.

The Main Zone input, analog or digital, is always routed through the Crystal decoder except during audio diagnostics. The serial audio interface consists of:

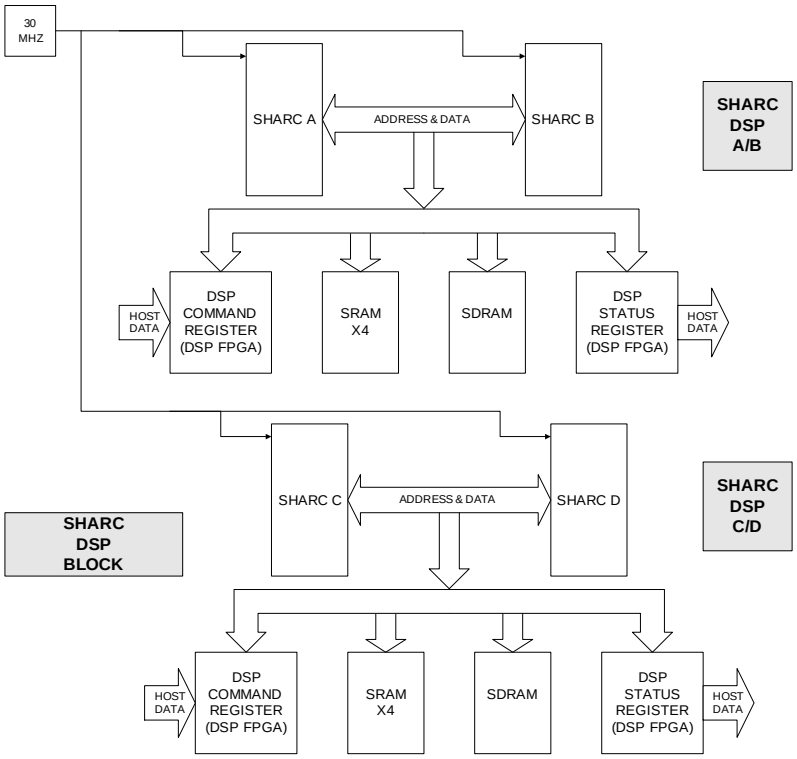
- DEC_SDI – 2 channel PCM audio stream input from either the Main Digital Receiver or the Main Analog ADC
- DEC_SDO(3:0) – four 2-channel PCM audio stream outputs that are routed down to the Audio FPGA on the main board where they are converted into octal data streams that are then sent to the Sharc DSPs
- DEC_IN_FSI – Input side word clock audio framing signal, 1 x input sample rate
- DEC_IN_SCKI – Input side audio bit clock, 64 x input sample rate
- DEC_OUT_FSI – Output side word clock audio framing signal, 1 x output sample rate
- DEC_OUT_SCKI – Output side audio bit clock, 64 x output sample rate.

It is possible for the input side of the CS49400 to run at half the sample rate of the output side. This is required for DTS 96/24 decoding.



DSP BOARD

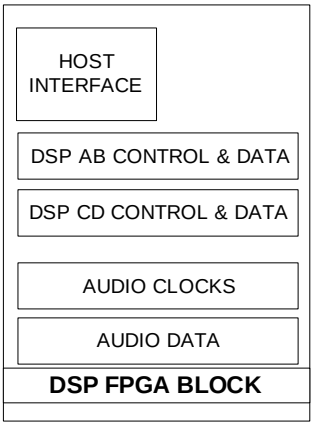
The principle DSP in the system consists of two pairs of Analog Device 21065 SHARC DSP engines, which reside on a daughter board. Each pair shares four 128kx8 12ns SRAMs and one 2Mx32 SDRAM. The SHARCs communicate with this external memory and each other over a 32-bit wide data bus. All necessary chip selects are generated by the SHARCs, including the clocking required for the Synchronous DRAM. The SHARCs master clock is provided by a 30MHz crystal oscillator that is distributed through a 74LCX14 inverter used as a buffer.



DSP Board FPGA

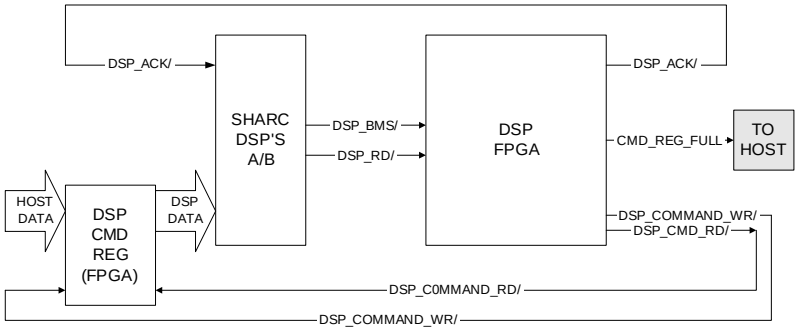
The DSP FPGA has a byte wide data path for the host interface with five-bits of addressing. It provides the following functions:

- Host communication with DSPs A, B, C and D. This includes resets, wait lines, status/control bits, data registers, and interrupts
- One GPIO bit from each DSP and one Flag bit common to all four
- Uses the FS/ and MCKI signals from the Audio FPGA on the main board to derive the necessary audio clocks – FS/ which is used as the sample interrupt, 4FS/ which is the octal frame sync and 256FS, the serial bit clock for the octal data stream.



Host Communication with the SHARC DSPs

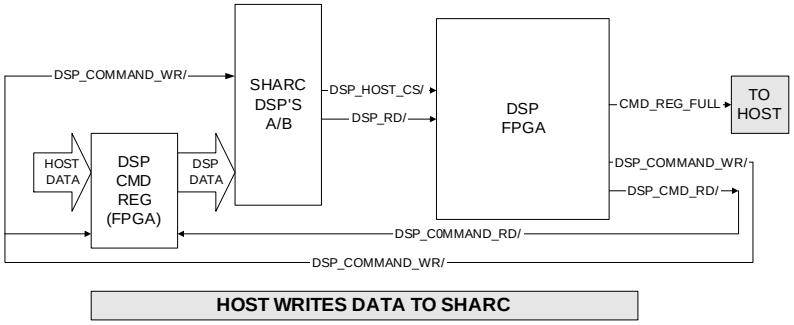
The lowest byte of the SHARC external data bus is also connected to the Host to DSP Command Register and the DSP to Host Status Register in the DSP FPGA. There are three modes of communication between the Host and the DSPs. The first occurs at boot time. When it comes out of reset, the A or C SHARC asserts DSP_BMS/ and DSP_RD/. These are combined by the DSP FPGA to create SP_CMD_RD/. This signal is used to generate the DSP_WAIT/ signal, which is re-clocked by the DSP_30MHZ to synchronize it to the SHARCs. It is then sent to the SHARC as DSP_AB_ACK where it keeps the SHARC in a wait state until the Z180 has written the data to the DSP Command Register.



HOST LOADS SHARC AFTER RESET: BOOT MODE

Host Writes Data to a SHARC DSP

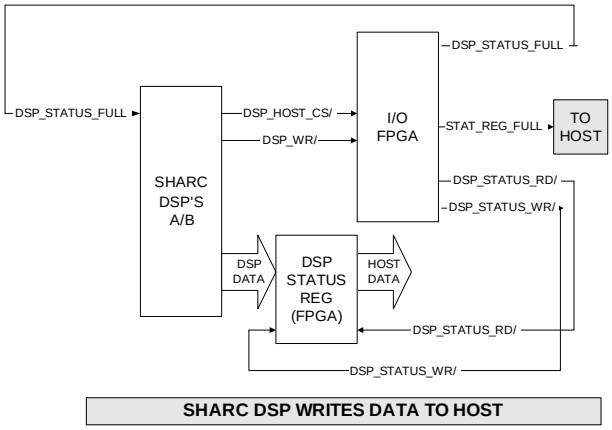
This is how the host transmits data to the SHARCs during run-time. The Host writes a byte to the DSP Command Register. The write strobe, **DSP_COMMAND_WR/** also interrupts the SHARC to let it know that a byte is waiting. The SHARC then retrieves the byte by asserting **DSP_HOST_CS/** and **DSP_RD/**. This also clears a status bit in the DSP FPGA, informing the host that the command register is empty and can be written to again.



HOST WRITES DATA TO SHARC

SHARC DSP writes Data to the Host

The SHARC writes a byte into the DSP to Host Status Register in the DSP FPGA by asserting DSP_HOST_CS/ and DSP_WR/. This sets a bit in the DSP FPGA that informs the host that that register is full and waiting to be read. When the host reads the byte, the DSP_STATUS_FULL line to the SHARC is cleared so the SHARC knows that the register is empty and can be written to again.



SHARC DSP WRITES DATA TO HOST

HOST-DSP COMUNICATIONS BLOCK

AUDIO ROUTING

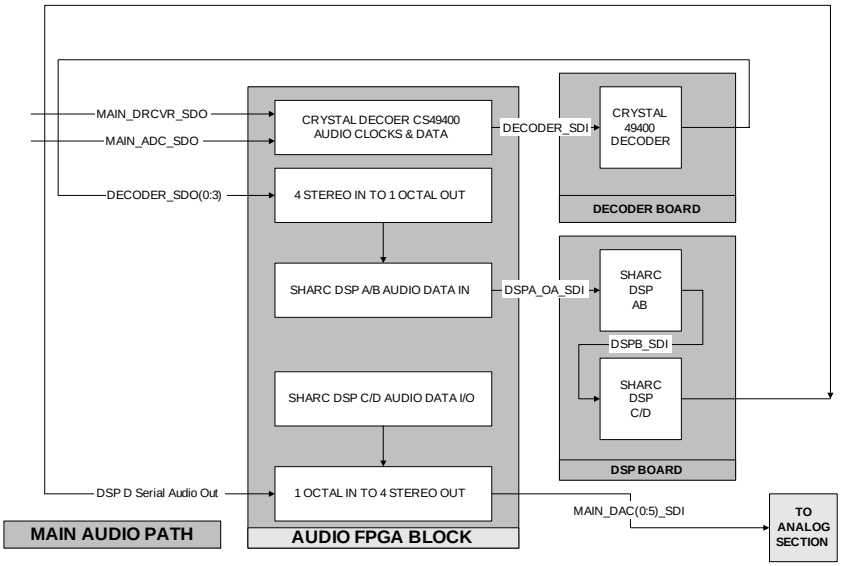
Digital Audio Input Path

Digital Audio can be either PCM 2-channel data or one of the compressed data formats. It enters the unit on one of the digital input connectors that are connected to the Audio FPGA. The FPGA functions as a mux and routes the output NRZ, (Non Return to Zero) data of the connector selected by the user to the two Digital Receivers, Main and Zone. These receivers lock to the incoming signal and extract a 2-channel PCM audio signal that is returned to the Audio FPGA.

Main Audio Data Path

The Main Audio Data Path is as follows:

1. Output of the Main Digital Receiver and the Main ADC to the Audio FPGA
2. Output of the Audio FPGA to the Crystal 49400 Decoder on the Decoder Board, Daughter Board 0
3. Four 2-channel outputs from the Crystal 49400 Decoder back to the Audio FPGA
4. The four 2-channel streams are packed into a single octal data stream in the Audio FPGA
5. The output of the octal packer is sent to SHARC A on the DSP Board
6. The octal output of SHARC B is sent to the input of Sharc C
7. Two octal outputs of SHARC D are sent back to the Audio FPGA on the Main board
8. The two octal outputs from SHARC D (not all slots are used) are unpacked into four 2-channel PCM streams in the Audio FPGA
9. These four 2-channel streams are sent to the Analog board as MAIN_DAC(0:4)_SDI.

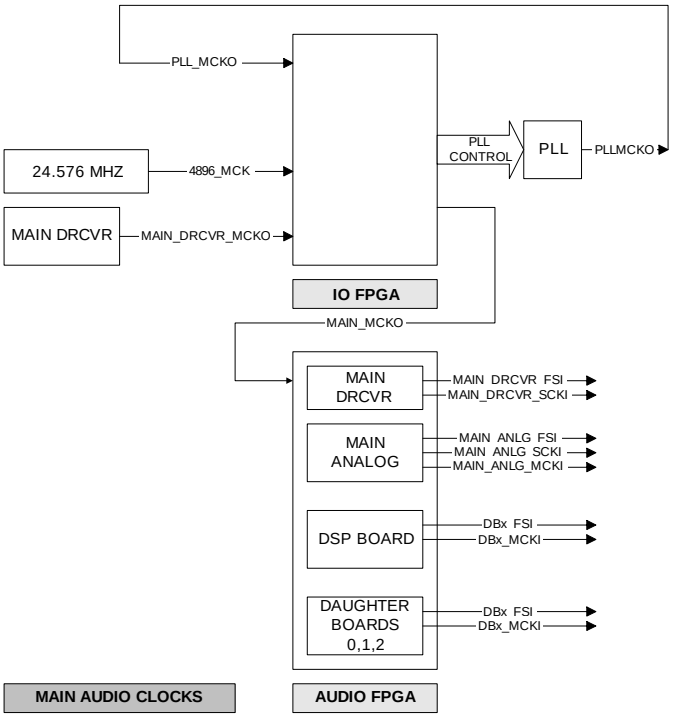


Main Audio Clock Path

There are two possible sources of master clock for the Main Audio Path. The 24.576 oscillator that can provide either a 48kHz or 96kHz sample rate, or the master clock output of the main digital receiver. In practice, the unit runs off the crystal at 96kHz when the input is analog. When the input is digital, the master clock output of the digital receiver is used. This master clock is de-jittered by the PLL that is controlled by the I/O FPGA using signals derived from **MAIN_DRCVR_MCKO**.

Depending on the input selected, the appropriate master clock is routed from the I/O FPGA to the Audio FPGA. Here it drives a clock tree that divides down the master clock, which is 256 times the sample rate, 256FS, to create the other clock rates required.

- The SHARC DSPs receive a word clock, or framing signal, FS and a bit clock of 256FS
- The Digital Receiver, ADCs and DACs use a word clock, FS/and bit clock, 64FS/
- The DSP and Decoder Boards receive a 256FS Master Clock and a word clock, FS/. These are used on each individual board to derive the audio clock signals required by that particular board.



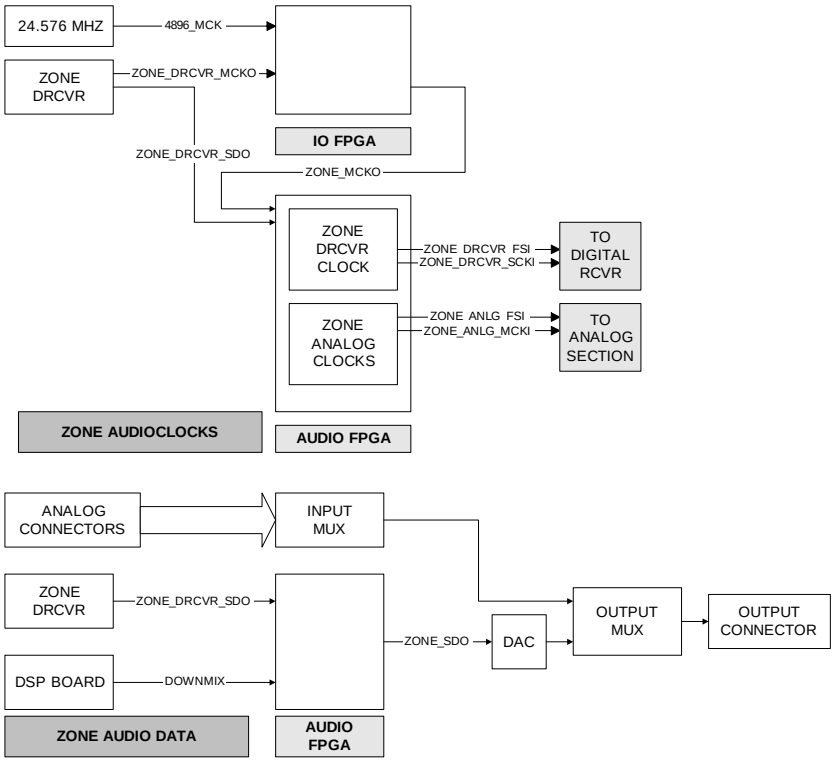
Zone Audio Clock and Data Paths

The Zone Audio Data Path is as follows:

- Output of the Zone Digital Receiver to the Audio FPGA
- A 2-channel stream is sent to the Analog section as **ZONE_DAC_SDI**. This stream is either the output of the Zone Digital Receiver or a 2-channel down-mix of the Main Audio content.

There are three possible sources of master clock for the Zone Audio Path. The 22.5792mHz crystal oscillator that provides either a 44.1kHz or 88.2kHz sample rate, the 24.576 oscillator that provides either a 48kHz or 96kHz sample rate, or the master clock output of the Zone digital receiver. In practice, the unit runs off the crystal at 96kHz when the input is analog. When the input is digital, the master clock output of the digital receiver is used. Depending on the input selected, the appropriate master clock is routed from the DAR FPGA to the Audio FPGA. Here it drives a clock tree that divides down the master clock, which is 256 times the sample rate, 256FS, to create the other clock rates required.

- The Digital Receiver uses a word clock, FS, and bit clock, 64FS
- The Analog Board receives a 256FS Master Clock and a word clock, FS. These are used on the analog board to derive the audio clock signals required by the devices on that board.



VCO BOARD OVERVIEW

The MC-8 VCO board is an isolated Voltage-Controlled Oscillator module that forms part of an overall PLL for generating master clocks for digital audio in the MC-8 system. The board is housed in a shielded enclosure and mounts to the main board through a 5-pin in-line header J1, which carries control-voltage input, oscillator output, and 5-volt power and ground. The VCO assembly is soldered to the MC-8 main board, which incorporates the phase-detector and error amplifier to form the complete PLL.

MC-8 ANALOG OVERVIEW

The analog section of the MC-8 encompasses all of the analog audio inputs and outputs, level controls and A/D and D/A converters. This section is located near the rear panel connections on the MC-8 Main Board. There are two separate signal paths: Main and Zone 2. Each of the eight analog stereo inputs or eight digital inputs can be routed to any of the two paths. The Main path digitizes the analog signal (if selected) and passes it to the DSP. Refer to the Main Audio Path 2-Channel Input block diagram in the next column. The DSP creates eight different output signals from the 2-channel input. D/A converter ICs convert each of the eight signals from the DSP to analog. The signals pass through level controls to their respective RCA connectors. A direct analog path is also provided which passes a 2-channel analog input signal directly to the Left and Right Front outputs via the level controls, bypassing the DSP and converters.

The MC-8 Balanced version offers additional Balanced Main and Zone 2 analog outputs using XLR connectors. In this version, an internal 34-pin ribbon cable routes the post level control signals from the Analog board to the XLR board. The XLR board incorporates active balanced output drivers for each of the ten outputs.

In addition, two 5.1-channel sources can be selected for the Main audio path. There are two possible methods of getting a 5.1-source into the box. Refer to the Main Audio Path 5.1-Channel Input block diagram above.

1. An S/PDIF signal may be encoded in Dolby Digital or DTS format and pass through a decoder that outputs the 5.1 channels. These channels are then passed along to the DSP.
2. Two sets of three separate analog input pairs can be routed directly to the outputs, bypassing the DSP and converters. This mode is available for DVD-Audio and multi-channel SACD players with 5.1 analog outputs. In the first case, Input 3 would pass to the Left and Right Front outputs; Input 4 would pass to the Center and Subwoofer outputs. Input 5 would pass to the Left and Right Side and Rear outputs. A duplicate set uses inputs 6, 7, and 8 in a similar manner.

Any of the eight analog or eight digital audio inputs can be selected as the source for the Zone 2 Audio Path as shown in the Zone 2 Audio Paths block diagram below. An analog source can be passed directly to the analog outputs. Likewise, a digital source can be passed directly to the digital outputs and be routed to a D/A converter for the analog outputs. In addition, a 5.1 Dolby Digital or DTS encoded 5.1 digital source may also be selected and passed through a decoder which will output a 2-channel downmix for the Zone 2 outputs. One S/PDIF RCA (coaxial) output port is available.

Analog Audio Inputs

The Left input jacks and associated circuitry are on the first sheet. See the second sheet for the Right input jacks and circuitry. Each input pair is buffered by a dual TL072 op amp. Each buffer connects to two DG408 8x1 CMOS switches. There are separate switches for the Main and Zone 2 analog source selection with independent switches for left and right channels, for a total of four DG408s.

The outputs of the Main source selectors feed the Main Input Level control. Two dual op amps are used for the direct analog path to the Front L/R outputs and the Zone 2 outputs and buffer a 6dB voltage divider that feeds the level control.

At the bottom right-hand corner of sheets one and two are two op amps. These amplifiers are used when routing a 5.1-analog source. One buffers the Center and Subwoofer signals from Inputs 4 or 7 while the other buffers the Surround L/R signals from Input 5 or 8.

Microphone Inputs and Main A/D Converter

Two microphone inputs are provided for use with an optional daughter card with 1/8-inch microphone connectors and preamplifiers. A DG411 analog switch can select Mic inputs 1 and 2 to be passed to the Main Input level control and A/D converter. When the Mic input is selected, the Analog inputs are disabled by bringing MAIN_ANLG_EN low.

The Main Input level control is the PGA2311, which has a range from +31.5 to –95.5 dB in 0.5 dB steps. The PGA2311 operates on ±5 volt rails and cannot handle signal levels greater than 7.5 Vpp.

Two dual op amps provide the left and right differential audio signals to the A/D converter. The op amp circuits bias the signals at 2.5 V and attenuate it by 7dB. This means a 2 Vrms signal at the output of the level control will be equivalent to 0 dBFS after the A/D conversion.

The AK5383 stereo A/D converter incorporates a dual-bit deltasigma architecture. It outputs 24 bits at a 96kHz sample rate under normal operation. The serial audio data from the A/D converter goes directly to the digital part of the Main board. The A/D also provides a signal to mute the Main analog inputs (MAININ_VC_MUTE/) when it is going through calibration during power up or sample rate changes. Control signals are used for reset (MAIN_ADC_RST/) and to place the converter in 88.2k or 96k sample rate mode (MAIN_ADC_96K_EN). The Audio FPGA (sheet 4) provides three clocks: MAIN_ADC_MCKI/, which is 256xFS for 44.1k and 48k sample rates, 128xFS for 88.2k and 96k sample rates; MAIN_ADC_SCKI/, which is 64xFS; and MAIN_ADC_FSI/ which is 1xFS (where FS = sample rate).

Zone 2 D/A converter

The AK4395 24-bit delta-sigma stereo D/A converter operates up to 192 kHz. The DAC is configured through its serial control port (pins 8,10,11) with a separate Reset pin.

The output of the DAC passes through a second order low-pass filter with its –3dB frequency at 83kHz. The filter is flat out to 20kHz. It has an overall gain of 7.4dB when measured at the test points. This means a 0 dBFS signal at the D/A converter will be 4Vrms going into the analog switches.

ADG451 analog switches select either the output of the respective DAC or the analog input source directly. The selected signal goes to the PGA2310 output level control and driver. These are special volume controls that run from +/-15 volt supplies and have a built-in op-amp driver. Zone 2 analog output has a maximum output level of 4 Vrms. The signal passes through a muting relay on the way to the output jacks. The relays are controlled by the ZONEOUT_MUTE/ signal.

Main D/A Converters

There are eight outputs for the Main Audio Path. The D/A circuitry is shown for two outputs on each sheet. The circuitry is identical for all eight outputs.

The AK4395 is the same 24-bit D/A converter that operates Zone 2.

The Analog FPGA (sheet 4) is the source for the clocks and data for the D/A converters. The MCLK is at 256 times the sample rate (FS). Each converter gets MCLK through a separate source resistor. The SCLK (64xFS) and LRCK (1xFS) are distributed to two sets of two DACs via separate source resistors. All of the D/A converters operate in I2S mode.

The AK4395 DACs are configured through their serial ports (pins 8,10,11). FRONT_DAC_RST/ puts the Front L/R pair of DACs into reset, while all other DACs share the same reset line (MAIN_DAC_RST/).

A second order low-pass filter follows the DACs. The filter amplifies the 1.7Vrms differential signal to 8Vrms (+13.5 dB) and converts it to single-ended for the level controls. Note these values assume a 0 dBFS digital input signal to the DAC. ADG451 analog switches are used to select either the DAC output or analog input for the respective output. These direct analog signal paths have been designed to support two modes:

- 2-channel analog direct or bypass mode. Any analog input can be routed directly to the L/R Front outputs
- 5.1-channel analog direct or bypass mode. When this mode is enabled, specific analog input signals are routed to specific analog outputs according to the table below.

Two different pairs of control bits are used to select the DSP/DAC signals or analog input signals for the Main outputs. FRONT_DACOUT_SEL/ selects the Front L/R DAC outputs for the Left and Right Front outputs when low. FRONT_DIRECT_SEL/ selects the analog input for the Front outputs. MAIN_DACOUT_SEL/ selects the respective DAC outputs for all of the other Main outputs (Center, Sub, L/R Side, L/R Rear) whereas MAIN_DIRECT_SEL/ selects the 5.1 analog inputs directly.

The output from the analog switch goes to a PGA2310 output level control and driver. This level control operates from +/-15V rails with a gain range from +31.5dB to –95.5dB in 0.5dB steps. Each PGA2310 controls a signal pair.

The outputs from the level control pass through DC-blocking caps and relays before going to the RCA connectors. The relays mute the Main outputs during a power cycle and whenever the unit is in Standby or Off. The relays are controlled by the MAINOUTS_MUTE/ signal.

The PGA2310 outputs also go to a 34-pin connector. This connector is used for routing the audio to the XLR board in MC-8 Balanced models.

Control Registers and XLR Board Connector

A 34-pin dual row ribbon connector routes the audio signals to the XLR board for MC-8 Balanced models. Five discrete 74HC273 control registers are located on the board. The Z180 writes to them via the 8-bit data bus (IODX_D[7:0]).

Control Register 0 provides the following:

- Mute relay control for the Main RCA outputs (MAINOUTS_MUTE/)
- Mute relay control for the Main XLR outputs (EXPOUTS_MUTE/)
- Mute relay control for the Zone RCA & XLR outputs (ZONEOUT_MUTE/)
- Mic selection
- 5.1 direct mux selection.

Control Register 1 provides the following:

- Analog source selection for the Main audio path (MAIN_ANLG_SEL[2:0]; MAIN_ANLG_EN)
- Main A/D calibration and 96kHz sample-rate enable (MAIN_AD_RST/; MAIN_AD_96K_EN).

Control Register 3 provides the following:

- Analog source selection for the Zone audio path (ZONE_ANLG_SEL[2:0]; ZONE_ANLG_EN)
- Zone DAC reset control (ZONE_DAC_RST/)
- Zone output selection – DSP or analog direct path (ZONE_DACOUT_SEL/; ZONE_DIRECT_SEL/)
- Mute for Zone output level control (ZONEOUT_VC_MUTE/).

Control Register 4 provides the following:

- Independent Zero crossing enable for each Main output level control (FRONT_VC_ZCEN, etc.)
- Zero crossing enable for the Zone output level control (ZONE_VC_ZCEN).

Control Register 6 provides the following:

- Main DACs reset control (MAIN_DAC_RST/)
- Main outputs selection – DSP or analog direct path (MAIN_DACOUT_SEL/; MAIN_DIRECT_SEL/)
- Mute for Main output level controls (MAINOUT_VC_MUTE/)
- Front Main DACs reset control (FRONT_DAC_RST/)
- Front Main output selection – DSP or analog direct path FRONT_DACOUT_SEL/;FRONT_DIRECT_SEL/)
- Mute for Front Main output level control (FRONT_VC_MUTE/).

Power Supply Connections and Regulators

There is a separate feed from the 60W switching power supply to the Analog section of the Main board. The Video board gets its power from the analog section. The Analog board has a 6-pin connector that accepts ±15 volts, ±5 volts and two ground connections to the supply. A 4-pin connector supplies the video board with +5VD, +5VA and –5VA.

A 7805 voltage regulator creates the +5VA supply from the +15V rail. Heat is dissipated by a heatsink. +5VA is an alternative "clean" 5-volt supply used by the A/D and D/A converters. +5VR is created in a similar way to provide a stable reference for the D/A converters.

MC-8 VIDEO SYSTEM CIRCUIT OVERVIEW

The MC-8 video section consists of two major functional blocks: video switcher and on-screen display (OSD) generator.

The video assembly consists of three boards, the Video RCA Board (schematic 060-15279), the Video Out Board (schematic 060-15339), and the Video Board (schematic 060-15269).

The RCA input and output boards connect to the main board via flexible ribbon connectors, with most of the active circuitry contained on the Video Board. Video input and output connectors are mounted directly on the boards, which attach to the rear panel of the MC-8. Separate cables supply power and control signals to the video assembly. Control from the main board is implemented via a serial interface.

Composite video inputs

Specific references are to input 1; other inputs are similar. Standard video levels applied to RCA jack J5 develop 1Vp-p is across 75-ohm termination resistor R15. Emitter-follower Q5 is located close to the connector and buffers the input with a gain slightly less than unity. Transistor bias is supplied through R13. Buffered video is fed to pin 10 of ribbon cable J6 through low-value series resistor R14, which reduces high-frequency peaking in the transmission path to the video board.

Composite video outputs

Composite video outputs originating on the video board are fed through individual pins of J3 to the corresponding output RCA jacks. The on-board traces are controlled-impedance and form part of a 75-ohm wideband transmission system, and output level is 1Vp-p when terminated in 75 ohms (2Vp-p open-circuit).

S-video inputs

Specific references are to input 1; other inputs are similar. S-video luminance inputs (pin 4 of the mini-din jacks) are terminated and buffered the same as composite inputs. AC-coupling is applied after buffering; C45 couples S-video #1 luminance. Chrominance input #1 (pin 3 of mini-din jack J13) is first ac-coupled by C42, and then buffered by emitter follower Q10. The dc-level at the chroma input pin is direct-coupled to subsequent sense circuitry through R80.

Main (Monitor) Composite / S-video

Composite and S-video luminance connect to multiplexers U17 and U18. S-video chrominance connects to U16. The composite multiplexer is addressed by the MVID_SELn bits, and the S-video multiplexers are addressed by the MSVID_SELn bits. When MCVID_EN/ is asserted low, U18 is enabled, and all MSVID_SELn bits are forced to 0 (U20, sheet 7). Composite multiplexer U18 selects one composite source. With MSVID_SELn set to 0, the S-video path is disabled because U17 is selecting a disconnected input, and U16 is selecting a grounded input to feed the chrominance channel. When MCVID_EN/ is high, U18 is disabled, disconnecting the composite inputs, and U20 passes addresses to the MSVID_SELn bits, allowing U17 and U16 to select one of the S-video sources.

The composite/luminance (MY) signal from U17/U18 is amplified by non-inverting stage U29. R164 makes the gain slightly greater than the desired factor of two in order to make up for slight losses in other stages. The signal from U29-1 is fed through R121 to the sync-stripper and dc-restorer. The dc-correction signal BPCOR returns through R166 to close the dc-feedback loop and maintain the video back-porch near 0Vdc. The signal OSD_Y_IN is distributed to output amplifiers U26 and U28, and also feeds the on-screen display.

Chroma selected by U16 (MC) is ac-coupled by C137 and amplified by U29, also with gain slightly greater than two. With a composite source selected, U16 is forced to input 0, grounding the chroma channel. The signal OSD_C_IN is distributed to output amplifiers U27 and U28, and also feeds the on-screen display.

The dc-level on the chroma channel of the selected source is fed to the base of Q15 through multiplexer U19 and the associated 100k series resistor. R132 raises the threshold for sensing a high level. The dc-amplifier formed by Q15 and Q14 is disabled when MORPHEN/ is high. When enabled, a high dc-level on the chroma input will drive base current into Q15. Q15 saturates and turns on Q14, which applies a high dc-level to the filter formed by R31 and C112. With low dc-level input, both transistors remain off, and no dc is fed to the filter. This circuit discriminates a low or high dc voltage on the selected chroma input and forms a 0 or 5V level accordingly. The sensing threshold is around 3V.

Main S-video at J2 is driven by gain-of-one amplifiers U26 (luma) and U27 (chroma). Internal multiplexers in these amplifiers determine whether the S-video is taken from the OSD path (MSTHRU/=hi) or straight through from the input amplifiers (MSTHRU/=low). MSTHRU/ follows MTHRU/ unless MSVID_OFF is asserted allowing main S-video luminance to be shut off when a composite source is in use. Amplifier outputs are fed through 75-ohm series resistors (R148, R151), forming a matched transmission- line driver system. R150 and R152 compensate for slight impedance errors due to the resistance of the on-board connecting traces. The chroma output is ac-coupled by C130, with a dc-level introduced through R3. When MORPHEN1/ is asserted low, switch U1 permits the main chroma output to follow the dc-sensing circuit.

Main composite video CVID_MAIN is driven by U28. Luma and chroma from the input amplifiers are summed by R162 and R159, scaled by 1/2. The result is amplified by U28, which has a gain of slightly more than two. With composite input, there is no chroma, and the result is simply the composite video. With S-video input, the result is the composite version of the S-video, the sum of Y+C. The internal U28 multiplexer selects whether the OSD is in the path or whether the input is fed straight through, controlled by MTHRU/. Output impedance is structured as with the main luma output.

Standard 1Vp-p video input levels produce 1Vp-p output on the composite and luminance channels when terminated in 75 ohms, or 2Vp-p open circuit. The composite main output is fed to the output RCA jack on the Video Out board via ribbon cable J16.

Zone Composite / S-video

Zone video circuitry is structured similarly to main video, but without OSD capability. Refer to the previous section for additional description. Multiplexers U11 and U10/U9 are addressed by the ZVID_SELn and ZSVID_SELn bits respectively to select an independent record source, but otherwise operate like their counterparts in the main path. There is no dc-restorer in the zone path, so back-porch dc-level varies with average picture level due to input ac-coupling. The multiplexer internal to output amplifier U13 allows the zone S-video luminance to be shut off when a composite source is in use. The zone composite output is fed to its RCA jack on the Video Out board via ribbon cable J16.

Component Video Switcher

Component video switching is performed by means of relays to maximize signal fidelity and format compatibility. There is no active circuitry in the component video path.

Three sets of component input RCA jacks (component inputs 1,2,3) feed a 3-wide, two-tier tree of double-throw relays. Each tier is comprised of a pair of dpdt relays. The tree selects one of the input sets and presents it to the bank of final output relays. The final tier of relays (RY3,RY1) connects the output RCA jacks to either the selected component source or to the OSD. One transistor driver is associated with each pair of relays. Relays are actuated when the associated PSELn bit is asserted high, switching from the normally closed to the normally open circuits.

Component OSD luminance (Y) is taken from the normal analog luminance output of the OSD chip. Color-difference signals (Pr, Pb) are derived from logic-level signals from the RGB port of the chip.

U5 buffers the logic levels and provides inverted versions of R and B. A resistor array forms a weighted sum of the RGB levels along with appropriate dc-offset and scaling to implement the standard color difference matrix: =

- Y= .587G+.299R+.114B
- Pr = .713 (R-Y)
- Pb =.564 (B-Y).

U6 serves as buffer/filter/output driver for the Pr and Pb and drives the outputs through series-terminating resistors R27, and R34.

One normally closed pole of RY5 grounds OSD_PY_OUT in order to effectively disable component output.

The signals generated by the MC-12 OSD are compatible only with the 480i component format. When incompatible formats are in use, the component OSD is inapplicable, and is not accessed by the operating system software.

On-Screen Display Signals

OSD chip U32 produces a character-based video display that can be overlaid on program video or that can occupy a full-screen, based on an independent internal video generator. OSD modes and parameters are controlled by an extensive set of internal registers, accessed via serial interface.

The character strings to be displayed are loaded serially into the screen memory within the chip. The bitmapped patterns that define the shapes of individual characters are stored in external font memory, interfaced through the A[15:0] and D[7:0] buses (see below). Character dot-clock is fixed at about 15 MHz, based on the external LC circuit formed by L1/C108/C109. Oscillator U33 (PAL) or U34 (NTSC) supplies a crystal clock. The active oscillator is determined by a high level on either NTSC_EN or PAL_EN, enabling the respective oscillator.

In overlay mode, composite or S-video luminance from the input amplifier is applied to YIN, and similarly, S-video chrominance (if applicable) is applied to CIN. The video applied to YIN is shifted to have a back-porch dc-level of about 1.57Vdc by U23 and associated circuitry. C101/C102 passively couple the ac-content of the luminance signal, with the op-amp providing the dc response. The chroma channel is biased to the same 1.57V level by R129/R130. The OSD video is related to program video by the separate H and V syncs (GMHSYN/, VSYNC/) derived by the sync stripper.

The full-screen mode is independent of video and sync inputs. Raster generation is based on the appropriate crystal clock.

The OSD luminance output is dc-shifted back to 0V back-porch level by U23 and associated circuitry. C98/C99 passively couple the ac-content, with the op-amp providing the dc response. Chroma is simply ac-coupled by C117/C125. The shifted OSD video is buffered and filtered by U24 to produce OSD_SY_OUT and OSD_SC_OUT. OSD_PY_OUT is buffered separately by U25 to drive the component osd luminance output. Switch U35 permits the S-video luminance to be turned off when MSVID_YOFF is asserted high. OSD_Y+C_OUT is formed as half the sum of the buffer outputs. These OSD output signals feed the output amplifiers as described earlier.

In order to produce usable overlays in the SECAM system, the OSD switching action is bypassed at high frequency through U35 and R146, preserving an attenuated version of the fm color carriers.

On-Screen Display Serial Control

The internal registers of the OSD are programmed serially from the main board in multiple 8-bit packets on VIDEO_DATA, accompanied by VIDEO_SCLK, operating at 1 MHz. During routine OSD updating, OSD_CS/ is fed through U35 as the OSD chip-select. Each logical transfer to the OSD chip consists of a pair of single byte transfers.

Sync Stripper / DC Restorer

Video from input amplifier U29 is fed through R121 to U2, which drives sync stripper U3 and the dc-restorer formed by switch U1 and op amp U2.

Sync stripper U3 accepts analog video and extracts vertical and horizontal sync, producing logic level VSYNC-OUT and AFC-OUT pulses respectively. A phase-locked loop based on ceramic resonator Y1 provides robust horizontal sync extraction even from noisy video sources. Pull-down resistors on the outputs improve the pulse waveshapes. Sections of U4 buffer and shape the pulses from U3. AFC-OUT is stretched by R15/C18 before buffering in order to meet the minimum width necessary for the OSD chip. Sections of U4 and the network formed by R9, R10, D2 and C12 form pulses that are aligned with video back porch. These pulses switch U1, which in combination with integrator U2, forms a sample-and-hold circuit that closes the feedback loop around the input video amplifier during back-porch time. This acts to

maintain the back-porch level at 0V. D1 limits the negative-going output of U2 in order to minimize the undesirable effects of unusual sync patterns inherent in the macrovision video copy-protection scheme.

Additional logic within U3 detects the presence of a valid video input. SYNC_DETECT is fed to the main board for use in OSD management. With video input absent, AFC_OUT free-runs at around 15kHz.

Video Control Registers

Control registers are implemented using shift registers as serial-to-parallel converters. U36, 37, and 38 are 8-bit shift registers which are cascaded to receive a 24-bit serial word. Each chip contains internal shift stages plus a set of output latches. The shift clock and data are VIDEO_SCLK and VIDEO_DATA, shared in common with the OSD. All VIDEO_DATA gets accumulated in the shift stages, but the 24 output latches are only updated on the rising edge of VIDEO_REG/, which acts as a chip-select for the control registers. All control bits are initialized to 0 at power-up by VIDEO_RST/.

Font Flash Programming Interface

Three additional shift registers are dedicated to the in-system programming of flash memory U31, which holds the bitmapped OSD font pattern. U22 is interfaced to the memory D[7:0] bus, and U21/U30 are interfaced to the A[15:0] bus.

The shift stages of U22, 21, and 30 receive VIDEO_SCLK and VIDEO_DATA, in common with the OSD and the video control register chips, and their serial-to-parallel transfers are clocked by OSD_CS/, in common with the OSD chip U32. However, in normal operation, the tri-state outputs of these chips are disabled so they do not drive the buses, and the only bus activity is the fetching of font patterns from U31 over the A[15:0], D[7:0] buses under the control of OSD U32. When necessary, the host processor on the main board manages the programming of the font flash memory by means of control-register bits OSD_TSC/ and VROM_WR/. In normal operation both bits are de-asserted (set high).

When OSD_TSC/ is asserted low, the bus interface of OSD U32 is disabled, and the bus interface of the three shift registers is enabled. U35 disconnects OSD_CS/ from U32, and the OSD chip select remains high due to internal pullup, so the OSD chip will be isolated from subsequent serial transfers involving OSD_CS/.

The host loads the shift registers with memory address and data patterns, which are transferred to the parallel holding registers on the rising edge of OSD_CS/. With the tri-state outputs enabled, address and data are driven onto the memory buses. Data is written to the flash rom when the host asserts VROM_WR/.

Digital Audio Input Ports

The Video board incorporates two optical S/PDIF connectors (CP1,CP2) and four coaxial S/PDIF connectors (J14,J15), with associated amplifiers (U7,U8). S/PDIF signals are fed to the main board via J19.

Power and Control Interface

J19 is the control and status interface to the host. J17 supplies power from a connector on the main board. The main video +5-volt rail is +5VV, a filtered version of system +5VD, which also supplies relay coils through FB1. The negative rail is -5VV, derived from the main board -5VA. The sync stripper U3 is specially powered from a well-regulated rail, +5VAS, derived from the main board +5VA.

CHAPTER 7 – PARTS LIST

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
Main Board Assembly					
022-14458	PL,MECH ASSY,VCO,MC12/B	1.000			J31
202-09794	RESSM,RO,0 OHM,0805	31.000			R102,108,113,118,123 R181,183,185,186,192 R194,196,197,202,313 R314,320-324,343,362 R365,383-388,410
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	2.000			R179,434
202-09871	RESSM,RO,5%,1/10W,1K OHM	43.000			R180,220-248,278 R280,284,290,294 R305,308,381,409 R414,431,432,437
202-09872	RESSM,RO,5%,1/10W,33 OHM	31.000			R328-333,335-341 R356-361,363,364 R368-377
202-09873	RESSM,RO,5%,1/10W,10K OHM	29.000			R3,5,7,9,11,13,15,17 R19,21,319,326,342 R378,392-401,408 R415,416,430,435
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	2.000			R252,254
202-09897	RESSM,RO,5%,1/10W,470 0HM	3.000			R309,311,412
202-09899	RESSM,RO,5%,1/10W,47 OHM	1.000			R204
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	10.000			R159-162,318,327 R379,380,433,436
202-10558	RESSM,RO,5%,1/10W,47K OHM	6.000			R52,53,205,258 R259,438
202-10559	RESSM,RO,5%,1/10W,100 OHM	59.000			R23-42,264,269-276 R279,281-283,285-289 R291-293,295-304,306 R307,352-355,417,418
202-10569	RESSM,RO,5%,1/10W,10 OHM	7.000			R47-51,191,251
202-10571	RESSM,RO,5%,1/10W,100K OHM	25.000			R128,129,132,133,136 R137,140,141,144,145 R148,149,152,153,156 R157,182,184,189,190 R193,195,200,201,440
202-10585	RESSM,RO,5%,1/4W,51 OHM	4.000			R208,209,214,215
202-10586	RESSM,RO,5%,1/4W,100 OHM	26.000			R2,4,6,8,10,12,14,16 R18,20,127,130,131 R134,135,138,139,142 R143,146,147,150,151 R154,155,158
202-10598	RESSM,RO,5%,1/10W,330 OHM	2.000			R249,250
202-10836	RESSM,RO,5%,1/4W,1K OHM	6.000			R166,167,170,171 R174,175
202-10890	RESSM,RO,5%,1/10W,220 OHM	18.000			R43,44,382,389-391 R413,419-429
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	1.000			R407
202-10948	RESSM,RO,5%,1/10W,390 OHM	1.000			R22
202-10949	RESSM,RO,5%,1/10W,1.2K OHM	4.000			R255,256,261,316
202-11041	RESSM,RO,5%,1/10W,680 OHM	1.000			R1
202-11071	RESSM,RO,5%,1/4W,75 OHM	1.000			R277
202-12836	RESSM,RO,5%,1/10W,2.7K OHM	2.000			R45,46
202-14792	RESSM,RO,5%,1/10W,56 OHM	23.000			R163,164,260,265-268 R310,312,325,334 R344-351,366,367 R402,404
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	2.000			R262,263
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	3.000			R206,207,317
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	4.000			R168,172,176,439
203-11083	RESSM,RO,1%,1/10W,49.9K OHM	8.000			R64,68,74,78,84 R88,94,98
203-11737	RESSM,RO,1%,1/10W,5.76K OHM	8.000			R66,71,76,81,86 R91,96,101
203-11741	RESSM,RO,1%,1/10W,18.2K OHM	1.000			R253
203-11993	RESSM,RO,1%,1/10W,357 OHM	4.000			R55,57,59,60
203-11996	RESSM,RO,1%,1/10W,6.49K OHM	8.000			R62,63,72,73 R82,83,92,93
203-11997	RESSM,RO,1%,1/10W,13.7K OHM	1.000			R315
203-12167	RESSM,RO,1%,1/10W,374 OHM	1.000			R178
203-12363	RESSM,RO,1%,1/10W,90.9 OHM	1.000			R177
203-12370	RESSM,RO,1%,1/10W,280 OHM	16.000			R65,67,69,70,75,77 R79,80,85,87,89,90 R95,97,99,100
203-12371	RESSM,THIN,1%,1/10W,2.74K OHM	4.000			R54,56,58,61

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	4.000			R212,213,218,219
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	1.000			R257
203-13131	RESSM,RO,1%,1/10W,8.45K OHM	3.000			R165,169,173
203-13133	RESSM,THIN,1%,1/10W,1.15K OHM	4.000			R103-106
203-13134	RESSM,THIN,1%,1/10W,1.00K OHM	4.000			R187,188,198,199
203-13537	RESSM,THIN,1%,1/10W,5.62K OHM	2.000			R210,216
203-13638	RESSM,THIN,1%,1/10W,2.49K OHM	2.000			R211,217
203-15479	RESSM,THIN,1%,1/10W,1.21K OHM	16.000			R107,109-112 R114-117,119-122 R124-126
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	16.000			C166,167,172,173 C178,179,184,185 C190,191,196,197 C202,203,208,209
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	5.000			C310,311,316,317,410
240-10758	CAPSM,ELEC,1uF,50V,20%,5.5mmH	2.000			C302,385
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	2.000			C56,59
240-12330	CAPSM,ELEC,2.2uF,35V,20%	11.000			C12,15,18,21,24,27 C30,33,36,39,415
240-13216	CAPSM,ELEC,22uF,16V,20%	3.000			C222,224,226
240-13217	CAPSM,ELEC,47uF,16V,20%	4.000			C248,249,301,303
240-13642	CAP,ELEC,47uF,25V,RAD,NPOL,6D	10.000			C11,14,17,20,23,26 C29,32,35,38
240-13803	CAP,ELEC,560uF,35V,RAD,LOW ESR	1.000			C402
240-15668	CAPSM,ELEC,330uF,6.3V,20%,105C	21.000			C98-113,119,129 C139,149,159
241-09798	CAPSM,TANT,10uF,10V,20%	6.000			C244,247,276,293 C329,403
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	27.000			C42,45,48,51,54,116 C121,123,126,131,133 C136,141,143,146,151 C153,156,161,163,250 C263,266,270,271 C336,341
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	9.000			C309,312,314,318,321 C323,325,327,409
244-11589	CAP,MYL,.068uF,63V,RAD,5%,BOX	2.000			C338,343
245-09291	CAPSM,CER,470pF,50V,COG,5%	1.000			C414
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	2.000			C411,412
245-10544	CAPSM,CER,220pF,50V,COG,5%	16.000			C69-71,73,77-79,81 C85-87,89,93-95,97
245-10561	CAPSM,CER,100pF,50V,COG,5%	4.000			C278,279,282,283
245-10562	CAPSM,CER,150pF,50V,COG,10%	42.000			C1-10,164,165,170 C171,176,177,182,183 C188,189,194,195,200 C201,206,207,212-215 C221,223,225,308,313 C315,319,320,322,324 C326,408
245-10588	CAPSM,CER,33pF,50V,COG,10%	1.000			C228
245-11592	CAPSM,CER,680pF,50V,COG,5%	4.000			C61-63,65
245-11594	CAPSM,CER,2200pF,50V,COG,5%	4.000			C114,115,267,274
245-11645	CAPSM,CER,.47UF,50V,Z5U,20%	3.000			C229-231
245-11949	CAPSM,CER,1500pF,50V,COG,5%	8.000			C124,125,134,135 C144,145,154,155
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	203.000			C13,16,19,22,25,28 C31,34,37,40,41,43 C44,46,47,49,50,52 C53,55,57,58,60,64 C66-68,72,74-76,80 C82-84,88,90-92,96 C117,118,120,122,127 C128,130,132,137,138 C140,142,147,148,150 C152,157,158,160,162 C168,169,174,175,180 C181,186,187,192,193 C198,199,204,205,210 C211,216-220,227 C232-243,245,246 C251-262,264,265,268 C269,272,273,275,277 C280,281,284-292 C294-300,304-307,328 C330,334,335,337,339 C340,342,344-384 C386-391,394-401 C404,413

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
270-00779	FERRITE,BEAD	14.000			FB1-10,20-22,24
270-06671	FERRITE CHOKE,2.5 TURN	4.000			FB29-32
270-09799	FERRITESM,CHIP,600 OHM,1206	6.000			FB11-15,23
270-11545	FERRITESM,CHIP,600 OHM,0805	9.000			FB16-19,25,26,28 FB33,34
270-13802	INDUCTORSM,24uH,20%,2.74A	1.000			L1
300-10509	DIODESM,1N914,SOT23	5.000			D29,33,42,46,60
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	18.000			D3-20
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	5.000			D28,30-32,61
300-11599	DIODESM,GP,1N4002,MELF	11.000			D1,2,24-27,36-38 D47,48
300-14286	DIODESM,SCHOTTKY,1A,SMB	2.000			D34,35
310-10510	TRANSISTORSM,2N3904,SOT23	2.000			Q7,9
310-10565	TRANSISTORSM,2N3906,SOT23	3.000			Q4,6,8
310-10566	TRANSISTORSM,2N4401,SOT23	3.000			Q1,2,5
310-15016	TRANSISTOR,MOSFET,30V,TO220	1.000			Q3
330-09889	ICSM,DIGITAL,74ACT04,SOIC	1.000			U55
330-10523	IC,HEX INVERTER,74HCU04,SOP	1.000			U57
330-12452	ICSM,DIGITAL,74VHCT244,SOIC	10.000			U62,67,68,70,71 U76,77,81,82,91
330-13865	ICSM,DIGITAL,74VHC04,SOIC	3.000			U44,58,88
330-13876	ICSM,DIGITAL,74VHC273,SOIC	7.000			U48-52,93,94
330-14247	ICSM,DIGITAL,74VHCT245,SOIC	7.000			U61,69,74,75,80 U95,97
330-14534	ICSM,DIGITAL,74VHCT541,SOIC	1.000			U92
330-15084	ICSM,DIGITAL,74LVC14A,SOIC	1.000			U53
340-00742	IC,LINEAR,7805 (LM 340 T-5)	1.000			U63
340-09244	ICSM,LINEAR,78LS05,5V REG,SOIC	1.000			U54
340-10502	ICSM,LIN,LF353,DUAL OPAMP,SOIC	9.000	02/19/03		U21-28,56
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	6.000			U30,34,39,43,46,47
340-10567	ICSM,LIN,MC34164,+5V MON,SOIC	1.000			U98
340-11575	ICSM,LIN,7805,+5V REG,TO263	1.000			U60
340-11597	ICSM,LIN,TL072,DUAL OPAMP,SOIC	9.000		02/19/03	U21-28,56
340-12936	ICSM,LIN,OPA2134,DU OP AMP,SO8	5.000			U11-15
340-13137	IC,LINEAR,LM2941CT,ADJ,TO-220	3.000			U36-38
340-14535	IC,LIN,1585A,3.3V REG,TO220	1.000			U96
340-15492	ICSM,LIN,PGA2310,VOL,15V,SOIC	5.000			U1-5
340-15493	ICSM,LIN,PGA2311,VOL,5V,SOIC	1.000			U35
340-15740	ICSM,LIN,LM56C,THERMO,LP,SOIC	1.000			U66
345-13138	ICSM,INTER,CS8414,RCVR,SOIC	2.000			U64,65
345-13140	ICSM,INTER,RS232 XCVR,+5V,SOIC	1.000			U29
346-10549	ICSM,SS SWITCH,DG408,SOIC	4.000			U32,33,41,42
346-14583	ICSM,SS SW,ADG451QUAD,1P1T,SOI	7.000			U6-10,31,40
350-13676	ICSM,CPLD,MC12,MEM,V1.00	1.000			U83
350-13854	ICSM,FPGA,XCS05XL-4,10X10,VQFP	1.000			U72
350-13863	ICSM,SRAM,32KX8,70NS,SOIC,20uA	1.000			U90
350-14540	ICSM,FPGA,XCS20XL-4,20X20,PQFP	1.000			U87
355-13829	ICSM,ADC,AKM5383,24b,96kHz,SOP	1.000			U45
355-14761	ICSM,DAC,AK4395,24BIT,VSOP	5.000			U16-20
365-13861	ICSM,uPROC,Z8S180,33MHz,PQFP	1.000			U84
365-14683	ICSM,uPROC,PIC16C54,MC12,V1.00	1.000			U89
390-13885	CRYSTAL OSCSM,29.491MHz,TRI	1.000			U85
390-14544	CRYSTAL OSCSM,24.576MHz,TRI,3V	1.000			U73
410-11639	RELAY,2P2T,DIP,5V,HI SENS	5.000			RY1-5
430-10419	LEDSM,INNER LENS,RED	3.000			D23,43,45
430-10420	LEDSM,INNER LENS,YEL	7.000			D21,49,51,52,54 D56,58
430-10421	LEDSM,INNER LENS,GRN	8.000			D22,41,44,50,53 D55,57,59
460-04598	BATTERY,LITH,3V@160mAH,HORIZ	1.000			BAT1
500-03620	CONN,EURO,C,ROW a+c,FEM	4.000			J34,36-38
500-13643	CONN,EURO,C,48P,abc,RECP,VERT	1.000			J48
510-03922	CONN,POST,100X025,HDR,6MCG	1.000			J35
510-10546	CONN,POST,079,HDR,4MC	1.000			J43
510-10745	CONN,POST,100X025,HDR,2MC,POL	2.000			J18,42
510-12319	CONN,D-SUB,9FCX2,STACKED,PCRA	1.000			J14
510-13146	CONN,HDR,.200,4MC,PCRA	1.000			J15
510-13149	CONN,RCA,PCRA,1FCGX2V,WH/RED,G	13.000			J1-13
510-13538	CONN,RCA,PCRA,1FCG,BLK,GND	1.000			J17
510-13877	CONN,POST,.100,HDR,2X5MCG,LP	1.000			J19
510-13887	CONN,POST,.100,HDR,2X13MCG,POL	1.000			J46
510-14079	CONN,POST,156X045,HDR,4MC,LOK	2.000			J29,45
510-14080	CONN,POST,156X045,HDR,6MC,LOK	1.000			J32
510-14890	CONN,POST,.100,HDR,2X17MCG,LK	2.000			J28,30
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	2.000			H/S 704-14452
704-06165	HEATSINK,TO220,.75X.5X.5,TAB	3.000			U36-38
704-14452	HEATSINK,TO220,MTTAB,NUT,1.45H	2.000			U63,96
710-15250	PC BD,MAIN,MC8	1.000		01/17/03	PICK REV 4 PC BOARD

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
710-15250	PC BD,MAIN,MC8	1.000	01/17/03		PICK REV 5 PC BOARD
Memory Board Assembly					
202-09873	RESSM,RO,5%,1/10W,10K OHM	1.000			R1
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	3.000			C5; C1,2 (IF U1 POP); C3,4 (IF U2 POP)
350-15741	ICSM,FLASH,16M,MC8,V1.00	1.000			U1 (TSOP pkg); (or U2 for SOIC pkg)
350-15742	IC,ROM,27C020,MC8,MEM,V1.00	1.000			U3
500-13644	CONN,EURO,C,48P,abc,PLUG,RA	1.000			J1
520-04999	IC SCKT,32 PIN,MACH,TIN	1.000			U3
710-15290	PC BD,MEM,MC8	1.000			PICK REV 0 PC BOARD
Video Board Assembly					
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	4.000			R88,91,94,97
202-09871	RESSM,RO,5%,1/10W,1K OHM	16.000			R1,15,43-45,50,51 R58,59,66,67,74,75 R82,83,131
202-09873	RESSM,RO,5%,1/10W,10K OHM	9.000			R3,7,10,12,16,117 R133,134,172
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	1.000			R2
202-10426	RESSM,RO,5%,1/10W,15K OHM	13.000			R18,35-42,106,150 R152,153
202-10558	RESSM,RO,5%,1/10W,47K OHM	4.000			R89,90,95,96
202-10571	RESSM,RO,5%,1/10W,100K OHM	12.000			R11,48,56,64,72,80 R112,116,119,140 R161,166
202-10573	RESSM,RO,5%,1/10W,470K OHM	11.000			R53,61,69,77,85 R118,167-171
202-10943	RESSM,RO,5%,1/10W,22K OHM	3.000			R6,13,14
202-10944	RESSM,RO,5%,1/10W,33K OHM	1.000			R132
202-10945	RESSM,RO,5%,1/10W,1.5K OHM	1.000			R5
202-10947	RESSM,RO,5%,1/10W,680K OHM	1.000			R4
202-10948	RESSM,RO,5%,1/10W,390 OHM	1.000			R8
202-11042	RESSM,RO,5%,1/10W,6.8K OHM	2.000			R98,102
202-11071	RESSM,RO,5%,1/4W,75 OHM	4.000			R86,87,92,93
202-12369	RESSM,RO,5%,1/10W,36K OHM	4.000			R109,114,158,164
202-13579	RESSM,RO,5%,1/10W,22 OHM	10.000			R49,52,57,60,65 R68,73,76,81,84
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	19.000			R27,34,46,47,54,55 R62,63,70,71,78,79 R99,100,105,147,148 R151,155
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	4.000			R19,24,25,32
203-10837	RESSM,RO,1%,1/10W,475 OHM	5.000			R9,101,121,146,149
203-10840	RESSM,RO,1%,1/10W,750 OHM	14.000			R29,31,104,107,110 R111,113,115,138 R143,157,160,163,165
203-10895	RESSM,RO,1%,1/10W,681 OHM	2.000			R135,141
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	8.000			R103,108,137,139 R144,145,159,162
203-11082	RESSM,RO,1%,1/10W,15.0K OHM	1.000			R20
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	5.000			R120,122,125,128,130
203-11726	RESSM,RO,1%,1/10W,301 OHM	2.000			R154,156
203-11730	RESSM,RO,1%,1/10W,1.37K OHM	2.000			R26,33
203-12198	RESSM,RO,1%,1/10W,2.15K OHM	5.000			R123,124,126,127,129
203-12298	RESSM,RO,1%,1/10W,30.1K OHM	1.000			R17
203-12838	RESSM,RO,1%,1/10W,29.4K OHM	1.000			R21
203-12897	RESSM,RO,1%,1/10W,976 OHM	4.000			R28,30,136,142
203-14789	RESSM,RO,1%,1/10W,61.9K OHM	1.000			R22
203-14790	RESSM,RO,1%,1/10W,11.8K OHM	1.000			R23
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	3.000			C87-89
240-10758	CAPSM,ELEC,1uF,50V,20%,5.5mmH	1.000			C6
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	10.000			C29,33,37,41,45 C140-144
240-11827	CAPSM,ELEC,10uF,16V,20%	8.000			C17,83-85,99,106 C125,139
240-13217	CAPSM,ELEC,47uF,16V,20%	3.000			C66,86,101
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	5.000			C50,51,55,56,100
245-09895	CAPSM,CER,10pF,50V,COG,10%	1.000			C109
245-10416	CAPSM,CER,1000pF,50V,COG,5%	3.000			C14,15,137
245-10544	CAPSM,CER,220pF,50V,COG,5%	2.000			C10,12
245-10561	CAPSM,CER,100pF,50V,COG,5%	2.000			C8,9
245-10588	CAPSM,CER,33pF,50V,COG,10%	4.000			C48,49,53,54
245-10972	CAPSM,CER,.068uF,50V,X7R,20%	1.000			C7
245-10975	CAPSM,CER,3300pF,50V,X7R,10%	1.000			C11

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
245-10976	CAPSM,CER,47pF,50V,COG,5%	3.000			C20,25,115
245-10977	CAPSM,CER,330pF,50V,COG,5%	1.000			C18
245-11625	CAPSM,CER,33pF,50V,COG,5%	1.000			C122
245-12070	CAPSM,CER,15pF,50V,COG,10%	1.000			C108
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	90.000			C1-5,13,16,21-23 C26-28,30-32,34-36 C38-40,42-44,46,47 C52,57-65,67-82 C90-98,102-105,107 C110-113,117-119,124 C126-132,134-136,138 C145-148
245-12524	CAPSM,CER,68pF,50V,COG,5%	1.000			C123
245-14762	CAPSM,CER,6.8pF,50V,COG,5%	1.000			C120
245-14763	CAPSM,CER,12pF,50V,COG,5%	4.000			C19,24,114,116
245-14764	CAPSM,CER,82pF,50V,COG,5%	1.000			C121
270-00779	FERRITE,BEAD	4.000			FB1-4
270-11289	INDUCTORSM,10uH,10%	1.000			L1
300-10509	DIODESM,1N914,SOT23	1.000			D2
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	5.000			D1,6-9
300-11599	DIODESM,GP,1N4002,MELF	3.000			D3-5
310-10510	TRANSISTORSM,2N3904,SOT23	11.000			Q1-10,15
310-10565	TRANSISTORSM,2N3906,SOT23	1.000			Q14
310-10566	TRANSISTORSM,2N4401,SOT23	3.000			Q11-13
330-09797	ICSM,DIGITAL,74AC04,SOIC	1.000			U5
330-10505	ICSM,DIGITAL,74HC02,SOIC	1.000			U4
330-10506	ICSM,DIGITAL,74HC595,SOIC	3.000			U21,22,30
330-10523	IC,HEX INVERTER,74HCU04,SOP	2.000			U7,8
330-10524	ICSM,DIGITAL,74HC08,SOIC	2.000			U12,20
330-15667	ICSM,DIGITAL,74HCT594,SOIC	3.000			U36-38
340-10502	ICSM,LIN,LF353,DUAL OPAMP,SOIC	2.000			U2,23
340-11495	ICSM,LIN,LT1229,VID OPAMP,SOIC	2.000			U24,29
340-13856	ICSM,LIN,EL4421C,VIDAMP,W/MUX	3.000			U13,26,27
340-14791	ICSM,LIN,EL4422C,VIDAMP,W/MUX	1.000			U28
340-15683	ICSM,LIN,AD8072,VIDAMPX2,SOIC	4.000			U6,14,15,25
345-10503	ICSM,INTER,NJM2229,SYNSEP,SOIC	1.000			U3
346-10507	ISCM,SS SWITCH,74HC4051,SOIC	7.000			U9-11,16-19
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	2.000			U1,35
350-15672	ICSM,FLASH,128KX8,5V,90NS,PLCC	1.000			U31
365-13288	ICSM,uPROC,MB90092,OSDC,PQFP	1.000			U32
390-10516	RESONATOR,CER,503KHz	1.000			Y1
390-13857	CRYSTAL,OSCSM,14.31818MHz,TRI	1.000			U34
390-13858	CRYSTAL,OSCSM,17.73448MHz,TRI	1.000			U33
410-11639	RELAY,2P2T,DIP,5V,HI SENS	6.000			RY1-6
510-13128	CONN,MINIDIN,4FC,PCRA,GND	7.000			J1,2,9-13
510-13148	CONN,RCA,PCRA,1FCGX2V,BLK,GND	2.000			J14,15
510-13840	CONN,OPTO,PCRA,TORX173,6Mbps	2.000			CP1,2
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.000			J17
510-15471	CONN,RCA,PCRA,1FCGX2V,GRN,GND	2.000			J5,8
510-15472	CONN,RCA,PCRA,1FCGX2V,RED,GND	2.000			J4,7
510-15473	CONN,RCA,PCRA,1FCGX2V,BLU,GND	2.000			J3,6
680-15469	CABLE,100,PLUG/SCKT,2X17C,2"L	1.000			J19
710-15260	PC BD,VIDEO,MC8	1.000			PICK REV 3 PC BOARD

Video RCA Board Assembly

202-09871	RESSM,RO,5%,1/10W,1K OHM	5.000			R1,4,7,10,13
202-13579	RESSM,RO,5%,1/10W,22 OHM	5.000			R2,5,8,11,14
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	5.000			R3,6,9,12,15
240-11827	CAPSM,ELEC,10uF,16V,20%	2.000			C13,14
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	12.000			C1-12
310-10510	TRANSISTORSM,2N3904,SOT23	5.000			Q1-5
510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	5.000			J1-5
510-13840	CONN,OPTO,PCRA,TORX173,6Mbps	2.000			CP1,2
680-15475	CABLE,FFC,20CX.1,CRMP,ST/RA,3"	1.000			J6
710-15270	PC BD,VIDEO RCA,MC8	1.000			PICK REV 2 PC BOARD

Video Out Board Assembly

510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	2.000			J1,2
680-15474	CABLE,FFC,4CX.1,CRMP,ST/RA,3"	1.000			J3
710-15330	PC BD,VIDEO OUT,MC8	1.000			PICK REV 1 PC BOARD

DSP Board Assembly

202-09794	RESSM,RO,0 OHM,0805	13.000			R4,18,19,21-24,43-48
202-09872	RESSM,RO,5%,1/10W,33 OHM	12.000			R6-17
202-09873	RESSM,RO,5%,1/10W,10K OHM	2.000			R3,36

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	2.000			R39,41
202-11073	RESSM,RO,5%,1/4W,270 OHM	9.000			R25-32,40
202-11496	RESSM,RO,0 OHM,1206	7.000			R20,33-35,37,38,42
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	96.000			C3-98
270-11545	FERRITESM,CHIP,600 OHM,0805	4.000			FB2-5
310-10510	TRANSISTORSM,2N3904,SOT23	1.000			Q1
330-13866	ICSM,DIGITAL,74VHC244,SOIC	1.000			U8
330-13882	ICSM,DIGITAL,74LCX14,SOIC	1.000			U3
350-12456	ICSM,SRAM,128KX8,12NS,3.3V,SOJ	8.000			U9-12,17-20
350-13854	ICSM,FPGA,XCS05XL-4,10X10,VQFP	1.000			U7
350-13879	ICSM,SDRAM,512KX32X4,3.3V,TSOP	2.000			U4,14
365-13860	ICSM,uPROC,ADSP21065,60MHz,PQF	4.000			U5,6,15,16
390-13886	CRYSTAL OSCSM,30.0MHz,TRI,3.3V	1.000			U2
430-10419	LEDSM,INNER LENS,RED	4.000			D3,4,7,8
430-10421	LEDSM,INNER LENS,GRN	5.000			D1,2,5,6,9
500-03619	CONN,EURO,R,96P,a+c,PLUG,VERT	1.000			J1
710-15300	PC BD,DSP,MC8	1.000			PICK REV 2 PC BOARD
Decoder Board Assembly					
202-09872	RESSM,RO,5%,1/10W,33 OHM	1.000			R5
202-09873	RESSM,RO,5%,1/10W,10K OHM	2.000			R2,3
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	2.000			R7,8
202-10599	RESSM,RO,5%,1/10W,3K OHM	1.000			R1
202-11073	RESSM,RO,5%,1/4W,270 OHM	1.000			R6
202-11496	RESSM,RO,0 OHM,1206	1.000			R4
205-14586	RESSM,NET,5%,ISOL,10KX4	4.000			RP1,2,5,6
205-15737	RESSM,NET,5%,ISOL,3.3KX4	2.000			RP3,4
241-09798	CAPSM,TANT,10uF,10V,20%	1.000			C27
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	1.000			C12
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	24.000			C1-11,13,14,17-26,28
245-12524	CAPSM,CER,68pF,50V,COG,5%	1.000			C15
245-13810	CAPSM,CER,1200pF,50V,COG,5%,08	1.000			C16
270-11545	FERRITESM,CHIP,600 OHM,0805	1.000			FB1
300-11599	DIODESM,GP,1N4002,MELF	1.000			D3
300-14286	DIODESM,SCHOTTKY,1A,SMB	1.000			D1
310-10510	TRANSISTORSM,2N3904,SOT23	1.000			Q1
340-13883	ICSM,LIN,LM2937,2.5V REG,TO263	1.000			U6
350-13854	ICSM,FPGA,XCS05XL-4,10X10,VQFP	1.000			U4
350-15491	ICSM,FLASH,512KX8,3V,200NS,TSO	1.000			U1
365-15490	ICSM,uPROC,DSP,CS49400,LQFP	1.000			U2
390-12076	CRYSTAL OSCSM,12.288MHz	1.000			U3
430-10421	LEDSM,INNER LENS,GRN	1.000			D2
500-04557	CONN,EURO,C,ROW a+c,MALE,RA	1.000			J1
710-15310	PC BD,DECODER,MC8/MC12	1.000			PICK REV 2 PC BOARD
Switch/LED Board Assembly					
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	8.000			R17-23,29
202-10597	RESSM,RO,5%,1/10W,180 OHM	2.000			R24,25
202-10599	RESSM,RO,5%,1/10W,3K OHM	2.000			R26,27
202-10945	RESSM,RO,5%,1/10W,1.5K OHM	9.000			R1-4,9-12,28
202-10948	RESSM,RO,5%,1/10W,390 OHM	8.000			R5-8,13-16
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	1.000			C1
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	6.000			C2-7
300-10509	DIODESM,1N914,SOT23	3.000			D17-19
310-10510	TRANSISTORSM,2N3904,SOT23	1.000			Q1
330-10372	ICSM,DIGITAL,74HC574,SOIC	4.000			U2-5
330-10537	ICSM,DIGITAL,74HC541,SOIC	1.000			U1
330-14244	ICSM,DIGITAL,74VHCT138,SOIC	1.000			U6
430-13639	LEDSM,BLU,30MCB,AX,ZBEND,2.5MM	8.000			D5-8,13-16
430-13888	LEDSM,RED,60MCD,AX,ZBEND,2.5MM	2.000			D20,21
430-14527	LEDSM,SYEL,250MCD,AX,ZBEND,2.5	9.000			D1-4,9-12,22
453-13899	SWSM,PBM,1P1T,6.2MMSQ,200GF	21.000			SW1-21
510-13145	CONN,POST,.100,HDR,2X7MCG,LP	2.000			J1,2
680-14083	CABLE,100,PLUG/SCKT,2X13C,2"L	.000			J3
710-15280	PC BD,SW/LED,MC8	1.000			PICK REV 1 PC BOARD
Standby Board Assembly					
430-13888	LEDSM,RED,60MCD,AX,ZBEND,2.5MM	1.000			D1
453-13899	SWSM,PBM,1P1T,6.2MMSQ,200GF	1.000			SW1
510-10546	CONN,POST,079,HDR,4MC	1.000			J1
710-15320	PC BD,STANDBY,MC8	1.000			PICK REV 0 PC BOARD

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
XLR Board Assembly					
202-10585	RESSM,RO,5%,1/4W,51 OHM	20.000			R7,10,17,20,27 R30,37,40,47,50 R57,60,67,70,77 R80,87,90,97,100
202-10943	RESSM,RO,5%,1/10W,22K OHM	20.000			R3,4,13,14,23,24 R33,34,43,44,53 R54,63,64,73,74 R83,84,93,94
202-10948	RESSM,RO,5%,1/10W,390 OHM	2.000			R1,2
203-12720	RESSM,THIN,1%,1/10W,2.94K OHM	20.000			R5,6,15,16,25,26 R35,36,45,46,55 R56,65,66,75,76 R85,86,95,96
203-13132	RESSM,THIN,1%,1/10W,3.01K OHM	40.000			R8,9,11,12,18,19,21 R22,28,29,31,32,38 R39,41,42,48,49,51 R52,58,59,61,62,68 R69,71,72,78,79,81 R82,88,89,91,92,98 R99,101,102
240-13642	CAP,ELEC,47uF,25V,RAD,NPOL,6D	20.000			C21,22,28,29,35,36 C42,43,49,50,56,57 C63,64,70,71,77,78 C84,85
240-13803	CAP,ELEC,560uF,35V,RAD,LOW ESR	2.000			C91,92
245-10562	CAPSM,CER,150pF,50V,COG,10%	20.000			C1-20
245-10587	CAPSM,CER,18pF,50V,COG,10%	30.000			C24-26,31-33,38-40 C45-47,52-54,59-61 C66-68,73-75,80-82 C87-89
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	20.000			C23,27,30,34,37 C41,44,48,51,55 C58,62,65,69,72 C76,79,83,86,90
270-00779	FERRITE,BEAD	20.000			FB1-20
270-06671	FERRITE CHOKE,2.5 TURN	2.000			FB21,22
300-11599	DIODESM,GP,1N4002,MELF	2.000			D1,2
310-10566	TRANSISTORSM,2N4401,SOT23	2.000			Q1,2
340-12936	ICSM,LIN,OPA2134,DU OP AMP,SO8	10.000			U1-10
410-11639	RELAY,2P2T,DIP,5V,HI SENS	10.000			RY1-10
510-10881	CONN,XLR,3MC,PCRA,SMALL	10.000			J1-10
510-14890	CONN,POST,.100,HDR,2X17MCG,LK	1.000			J11
620-12428	LUG,#4,INT STAR,XLR GND	10.000			J1-10
710-15340	PC BD,XLR,MC8B	1.000			PICK REV 0 PC BOARD
IR/Encoder Board Assembly					
202-00528	RES,CF,5%,1/4W,820 OHM	1.000			R1
202-00530	RES,CF,5%,1/4W,1.2K OHM	1.000			R2
202-00531	RES,CF,5%,1/4W,1.5K OHM	1.000			R3
245-03609	CAP,CER,.1uF,50V,Z5U,AX,80/20%	2.000			C1,2
345-14780	IC,INTER,GP1U28,38kHz,IR DET	1.000			U1B
430-10594	LED,T1-3/4,IR	1.000			D1
430-14487	LED,T1,BLU,430NM	1.000			SYSTEM ON D4
430-14787	LED,T1,RED,700NM	1.000			OVERLOAD D2
430-14788	LED,T1,YEL,585NM	1.000			IR ACK D3
452-13640	SW,RTY,ENC,24POS,INC B,25L,VRT	1.000			SW1
630-14778	SPCR,LED,T1,.375"H	3.000			D2-4
680-14082	CABLE,100,PLUG/SCKT,2X7C,3"L	1.000			IR/ENC BD (J1) TO SW/LED BD
710-13690	PC BD,IR/ENC,MC12	1.000			PICK REV 2 PC BOARD
VCO Assembly					
700-14838	HOUSING,VCO,MC12	1.000			
700-14839	COVER,VCO,MC12	1.000			
202-09899	RESSM,RO,5%,1/10W,47 OHM	1.000			R1
245-09895	CAPSM,CER,10pF,50V,COG,10%	1.000			C3
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	4.000			C1,2,4,5
270-11545	FERRITESM,CHIP,600 OHM,0805	1.000			FB1
270-14359	COILSM,VAR,1uH,5%,5.6X6.2X6MM	1.000			L1
300-13881	DIODESM,VARACTOR,BB132	1.000			D1

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
340-14528	ICSM,LIN,MC100EL1648,VCO,SOIC	1.000			U1
– or –					
340-16132	ICSM,LIN,MC100EL1648,VCO,TSSOP	1.000			U1
510-14836	CONN,POST,100X025,HDR,5MC,RA	1.000			J1
710-14840	PC BD,VCO,MC12	1.000			PICK REV 0 PC BOARD
– or –					
710-16130	PC BD,VCO,MCLK	1.000			PICK REV 0 PC BOARD

Chassis Assembly

*Note: *items are on MC-8 only; ^items are on MC-8B only*

120-09621	ADHESIVE,THRDLOCK,GP	0.003			DSUB JSCKT
490-13144	CONN,PLUG,.200,4FC,RA,12-30G	1.000			REAR PANEL
527-12974	CONN,DSUB,JSCKT,4-40,.187X.25	4.000			DCONN TO R.PANEL
540-02472^	PLUG,HOLE,3/8",BLK	4.000			
541-15458*	FOOT,1.97X.43H,ABS,BLK	4.000			CHASSIS
635-13637	SPCR,M3X34MM,M/F,6MM HEX	2.000			VIDEO BD TO MAIN BD
635-14779	SPCR,M3X14MM,6MM HEX	2.000			MEM BD TO CHASSIS; DECODER TO CHASSIS
635-15468	SPCR,M3X16MM,M/F,6MM HEX	4.000			DSP BD TO MAIN BD
640-10467	SCRW,M3X6MM,FH,PH,BZ	2.000			PS SPT TO CHASSIS
640-10467	SCRW,M3X6MM,FH,PH,BZ	2.000			MEM BD TO CHASSIS; DECODER TO CHASSIS
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			PS SPT TO CHASSIS
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.000			MAIN BD TO CHASSIS
640-10498	SCRW,M3X6MM,PNH,PH,BZ	3.000			F.PANEL TO CHASSIS
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.000			DSP BD TO MAIN BD
640-10498	SCRW,M3X6MM,PNH,PH,BZ	5.000			VIDEO ASSY TO R.PNL
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			VIDEO ASSY TO MAINBD
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			MEM BD TO CHASSIS; DECODER TO CHASSIS
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.000			OPT PANELS TO REAR
640-10499^	SCRW,M3X8MM,PNH,PH,BZ	2.000			XLR BD TO 1U CHASSIS
640-13645	SCRW,M4X10MM,FH,SCKT,BZ	13.000			COVER TO CHASSIS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	2.000			F.PANEL TO CHASSIS
640-15476^	SCRW,M4X8MM,PNH,PH,ZN	3.000			1U FP TO 1U CHASSIS
640-15476^	SCRW,M4X8MM,PNH,PH,ZN	4.000			1U CHAS TO 2U CHAS
640-15477*	SCRW,M4X12MM,PNH,PH,ZN	4.000			FEET TO CHASSIS
641-01703*	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	2.000			ACCESS PANEL TO CHAS
641-10989	SCRW,TAP,AB,4X3/8,PNH,PH,BZ	6.000			R.PANEL TO CHASSIS
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	14.000			RCA CONN TO R.PANEL
641-14898^	SCRW,TAP,#4X1/4,PNH,PH,BZ,TRI	20.000			XLR BD TO 1U CHASSIS
680-14494^	CABLE,.10,SCKTX2-180,2X17C,6"	1.000			XLR (J11) TO MN (J28)
680-14539	CABLE,HSG/HSG,4C,4"	1.000			MN(J29) TO VID(J17)
680-15470	CABLE ASSY,3.5mmJACK/HSG,2C,3"	1.000			IR CONN TO MAIN BD (J18); DRESS NUT SUPPLIED W/JACK
700-15447	CHASSIS,2U,MC8	1.000			
700-15448	COVER,2U,MC8	1.000			
700-15450^	CHASSIS,1U,MC8B	1.000			
702-15444	PANEL,REAR,MC8	1.000			
702-14454^	PANEL,FRONT,1U,MC12B	1.000			
702-14495*	PANEL,ACCESS,MC12	1.000			CHASSIS BOTTOM
702-15457	PANEL,OPTION,BLANK,MC8	2.000			REAR PANEL
720-13632^	PAD,FOOT,1.438DIA	4.000			1U CHASSIS BOTTOM
720-15256	TAPE,COPPER,1/2"W,EMBOSSED,PSA	16.500			APPLY TO R.PNL TOP
740-14888	LABEL,LIC/PAT/WARN,MC12	1.000			MC8: 2U CHASSIS BOTTOM; MC8B: 1U CHASSIS BOTTOM

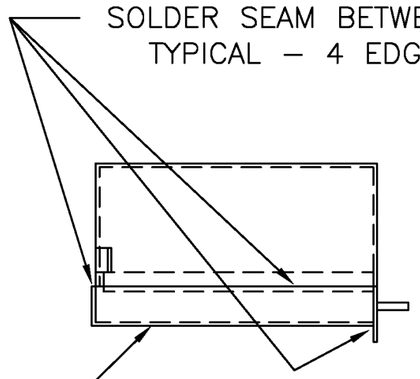
PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
Mic Board Assembly					
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	8.00			R41,50,52 R14,16,28,30,39
202-09871	RESSM,RO,5%,1/10W,1K OHM	1.00			R17
202-10426	RESSM,RO,5%,1/10W,15K OHM	4.00			R27,38,49,60
202-10598	RESSM,RO,5%,1/10W,330 OHM	4.00			R15,29,40,51
202-11073	RESSM,RO,5%,1/4W,270 OHM	4.00			R26,37,48,59
203-11077	RESSM,RO,1%,1/10W,237 OHM	1.00			R20
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	16.00			R18,19,21,22,31-3 R42-45,53-56
203-12481	RESSM,RO,1%,1/10W,1.50K OHM	1.00			R23
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	4.00			R25,36,47,58
203-12723	RESSM,THIN,1%,1/10W,102 OHM	4.00			R24,35,46,57
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	4.00			C8,14,20,28
240-11827	CAPSM,ELEC,10uF,16V,20%	12.00			C11-13,17-19,23-2 C31-33
240-13216	CAPSM,ELEC,22uF,16V,20%	1.00			C7
245-10562	CAPSM,CER,150pF,50V,COG,10%	8.00			C34,35,41,42,46,4 C51,52
45-10976	CAPSM,CER,47pF,50V,COG,5%	12.00			C38-40,43-45,48-5
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	13.00			C9,10,15,16,21,22 C30,36,37,56-58
270-11545	FERRITESM,CHIP,600 OHM,0805	9.00			FB3-10,13
300-11599	DIODESM,GP,1N4002,MELF	2.00			D9,10
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	4.00			U18-20,26
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1.00			U12
346-14583	ICSM,SS SW,ADG451QUAD,1P1T,SOI	1.00			U25
500-04557	CONN,EURO,C,ROW a+c,MALE,RA	1.00			J3
510-10595	PHONE JACK,3.5MM,PCRA,3C,STER	4.00			J5-8
640-10498	SCRW,M3X6MM,PNH,PH,BZ	4.00			2 PER BRKT
680-15743	CABLE,100,PLUG/SCKT,2X5C,2.5"L	1.00			J4
701-15738	BRACKET,MTG,MIC/DSP BD,MC8	1.00			PHONE JACKS
701-15739	BRACKET,MTG,OPT BD	1.00			
710-15380	PC BD,MIC/DSP,MC8	1.00			PICK REV 1 PC BOARD
740-11287	LABEL,S/N,PCB,PRIN	1.00			
Power Supply Assembly					
454-13850	SW,ROCKER,2P1T,5A/80A@250,TV5	1.000			
490-11462	CONN,AC,3MC,SNAP,04TH,IEC,10A	1.000			
530-02488	TIE,CABLE,NYL,.14"X5-5/8"	2.000			FERRITE SLEEVE TO PS SPT
640-10467	SCRW,M3X6MM,FH,PH,BZ	2.000			PWR SW TO PS SPT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			PWR SUP TO PS SPT
640-12534	SCRW,M3X20MM,PNH,PH,BZ	4.000			FAN TO PS SPT
643-10492	NUT,M4X.7MM,KEP,ZN	1.000			CHASSIS GND
644-01737	WSHR,LOCK,SPLIT,#4	2.000			PWR SUP TO PS SPT
644-02716	WSHR,FL,#4CLX.312ODX.03THK	2.000			PWR SUP TO PS SPT
644-10494	WSHR,FL,M4CLX9ODX.8MM THK	1.000			CHASSIS GND
680-11461	WIRE,18G,G/Y,2.5",187QDC/LUG#8	1.000			AC CONN TO CHAS GND
680-14536	CABLE,PWR,.187/.110QDC,SLV,4.5	1.000			AC CONN TO PWR SW
680-14537	CABLE,PWR,HSG/.110QDC,2C,5"	1.000			PWR SW TO PWR SUP
680-15465	CABLE,HSG/HSG,8C,SLV,16/17"	1.000			PWR SUP TO MAIN BD (J32 & J45)
700-15449	SUPPORT,PS,MC8	1.000			
720-14852	GASKET,FAN,1.5D/1.7SQ,BLK	1.000			FAN TO PS SPT
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1.000			PS SUPPORT
740-15745	LABEL,FUSE,CAUTION,2.5A/250V	1.000			PS SUPPORT
750-15466	PWR SUP,+-5V/+-15V,60W	1.000			
Fan Assembly					
410-14851	FAN,40X40X10MM,12VDC,3.43CFM	1.000			
525-12536	CONN,CONT,CRIMP,22-26AWG,AMP	2.000			CRIMP CONN TO WIRES
527-12537	CONN,HSG,CRIMP,.100X2,POL,LK	1.000			
Front Panel Mechanical Assembly					
550-15459	KNOB,1.75X.91H,6MM,ALUM,PEWTER	1.000			ENCODER
702-15440	PANEL,FRONT,MC8	1.000			
023-14068	PL,IR/ENC BD ASSY,MC12/B	1.000			
023-15437	PL,SW/LED BD ASSY,MC8/B	1.000			
023-15438	PL,STANDBY BD ASSY,MC8/B	1.000			
430-13143	DISPLAY,VF,20X2 CHAR,5X8DOT	1.000			
530-09382	CLIP,WIRE HRNS,.15DIA,ADH BAK	1.000			FP SHIELD,CENTER
550-13633	BUTTON,.276X.572,BLK	2.000			
550-13634	BUTTON,.276X.572,BLK,W/LTPIPE	20.000			

PART NO	DESCRIPTION	QTY	EFFECT.	INACT.	REFERENCE
635-14526	SPCR,M3CLX6MM,6MMRD	1.000			IR/ENC BD
640-01841	SCRW,2-56X1/4,PNH,PH,ZN	4.000			DISPLAY TO FP
640-10495	SCRW,M3X12MM,PNH,PH,ZN	1.000			IR/ENC BD
640-10498	SCRW,M3X6MM,PNH,PH,BZ	9.000			SHIELD TO FP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	6.000			SW/LED BD TO FP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			STANDBY BD TO FP
640-15476	SCRW,M4X8MM,PNH,PH,ZN	2.000			SPT BRKT TO FP
680-14693	CABLE,100,PLUG/SCKT,2X7C,10.5"	1.000			DSPLY TO SW/LED(J1). SOLDER TO DSPLY.
680-14854	CABLE,079,SCKT/SCKT,4C,4",CMP	1.000			STANDBY BD (J1) TO MAIN BD (J43)
701-15454	BRACKET,SUPPORT,COVER,MC8	1.000			
701-15456	SHIELD,6.5X1.8X.4"H	1.000			
703-14098	LENS,6.36X1.55,MC12	1.000			
Video Mechanical Assembly					
023-15431	PL,VIDEO BD ASSY,MC8/B	1.000			
023-15432	PL,VIDEO RCA BD ASSY,MC8/B	1.000			
023-15433	PL,VIDEO OUT BD ASSY,MC8/B	1.000			
635-15716	SPCR,M3X17MM,6MM HEX	1.000			VID RCA TO VIDEO
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	3.000			VIDEO BD TO BRKT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	2.000			VID RCA TO VIDEO
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	15.000			VIDEO BD TO BRKT
701-15455	BRACKET,VIDEO BD,MC8	1.000			
Packaging/Miscellaneous					
022-15306	PL,KIT,ACCESS PKG,MC8/B	1.000			
070-15039	NOTES,RELEASE/ERRATA,MC8	1.000			
070-15481	GUIDE,USER,MC8/B	1.000			
460-08345	BAT,ALK,AA	2.000			
730-11459	BOX,21X5X19,LEXICON	1.000			SHIPMENT
730-15286	BOX,17.75X12.125X2.5"	1.000			
730-15484	BOX,21-3/4X19X9-3/4,LEXICON	1.000			INNER BOX
730-15486	BOX,22-1/2X19-3/4X11,BLANK	1.000			OUTER BOX
730-14896	INSERT,FOAM,ENDCAP,1U,MC12B	2.000			
730-15487	INSERT,FOAM,BASE,2&3UX15	1.000			
730-15488	INSERT,FOAM,TOP,2&3UX15	2.000			
730-15483	TRAY,ACCESSORY,MC8/B	1.000			
750-15480	REMOTE CONTROL,MC8	1.000			
Power Cord Options					
680-09149	CORD,POWER,IEC,10A,2M,NA,SVT	1.000	N.AMER		
680-08830	CORD,POWER,IEC,6A,2M,EURO	1.000			
680-10093	CORD,POWER,IEC,5A,2M,UK	1.000			
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1.000			
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1.000			
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1.000			
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1.000			
Mounting Option					
630-08670	WSHR,FIN,#10,NYL,BLK	4.000			
640-08671	SCRW,10-32X3/4,FH,PH,BLK	4.000			
640-14680	SCRW,M4X14MM,FH,SCKT,SS	6.000			
701-15453	BRACKET,MTG,RACK,2U,MC8	2.000			
MC-8 to MC-8B Upgrade Option					
023-15439	PL,XLR BD ASSY,MC8B	1.000			
540-02472	PLUG,HOLE,3/8",BLK	4.000			
640-10499	SCRW,M3X8MM,PNH,PH,BZ	2.000			XLR BD TO 1U CHASSIS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	3.000			1U FP TO 1U CHAS
640-15476	SCRW,M4X8MM,PNH,PH,ZN	4.000			
641-14898	SCRW,TAP,#4X1/4,PNH,PH,BZ,TRI	20.000			XLR BD TO 1U CHASSIS
680-14494	CABLE,.10,SCKTX2-180,2X17C,6"	1.000			XLR BD (J11)
700-15450	CHASSIS,1U,MC8B	1.000			
702-14454	PANEL,FRONT,1U,MC12B	1.000			
720-13632	PAD,FOOT,1.438DIA	4.000			1U CHASSIS BOTTOM

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD ASSEMBLY SEQUENCE, CHG BOM NO. PER DCR #010109-01	AN 1/11/01 RL 1/17/01 WH 1/17/01	CW 1/17/01 KB 1/17/01
2	ADD 023-16129 VCO ASSY PER ECO #030314-00	AN 5/5/03 CLC 5/8/03	CW 5/9/03 KAB 5/12/03

STEP 5

SOLDER SEAM BETWEEN COVER & HOUSING
TYPICAL – 4 EDGES



STEP 3

INSTALL COVER
#700-14839
ONTO HOUSING

STEP 4

SOLDER BOX SEAMS
TYPICAL – 4 CORNERS

STEP 1

SOLDER BD ASSY
TO HOUSING
#700-14838
AT TAB

STEP 2

SOLDER 2 PINS
TO HOUSING

0.07 [1.8MM] MIN LENGTH
OF PIN TO BE FREE OF SOLDER

VCO BD ASSY
#023-14837
OR
#023-16129

NOTES

1. PART NO.'S SHOWN FOR REFERENCE ONLY SEE BOM #022-14458.
2. STEPS 4 & 5: ALL HOUSING SEAMS & SEAMS BETWEEN THE COVER & HOUSING ARE TO BE SOLDERED PER PCB WORKMANSHIP STANDARDS. JOINTS SHOULD BE SMOOTH AND NEAT WITH NO EXCESS BUILDUP.

	PCM-96
	RV-8
	MC-12/8
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME
14834-2

APPROVALS		DATE
DRAWN	AN	11/13/00
CHECKED	RL	11/13/00
Q.C.	CW	11/13/00
ISSUED	KB	11/13/00

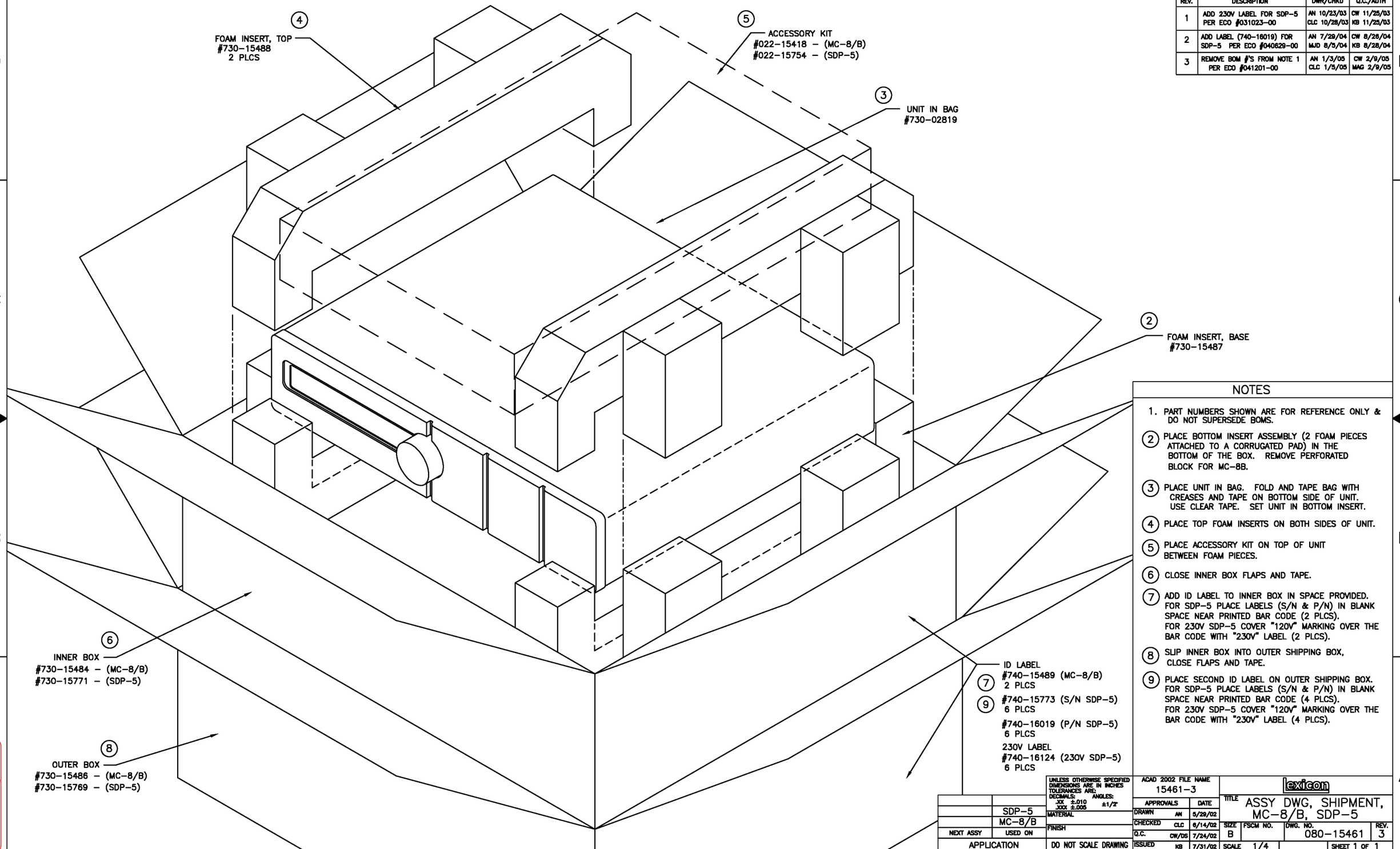
lexicon

TITLE
ASSY DWG, MECH,
VCO, MCLK

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14834	2

SCALE 2/1 SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD 230V LABEL FOR SDP-5 PER ECO #031023-00	AN 10/23/03 CLC 10/28/03	CW 11/25/03 KB 11/25/03
2	ADD LABEL (740-16019) FOR SDP-5 PER ECO #040629-00	AN 7/29/04 MJD 8/5/04	CW 8/28/04 KB 8/28/04
3	REMOVE BOM #'S FROM NOTE 1 PER ECO #041201-00	AN 1/3/05 CLC 1/5/05	CW 2/9/05 MAG 2/9/05



NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY & DO NOT SUPERSEDE BOMS.
2. PLACE BOTTOM INSERT ASSEMBLY (2 FOAM PIECES ATTACHED TO A CORRUGATED PAD) IN THE BOTTOM OF THE BOX. REMOVE PERFORATED BLOCK FOR MC-8B.
3. PLACE UNIT IN BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM SIDE OF UNIT. USE CLEAR TAPE. SET UNIT IN BOTTOM INSERT.
4. PLACE TOP FOAM INSERTS ON BOTH SIDES OF UNIT.
5. PLACE ACCESSORY KIT ON TOP OF UNIT BETWEEN FOAM PIECES.
6. CLOSE INNER BOX FLAPS AND TAPE.
7. ADD ID LABEL TO INNER BOX IN SPACE PROVIDED. FOR SDP-5 PLACE LABELS (S/N & P/N) IN BLANK SPACE NEAR PRINTED BAR CODE (2 PLCS). FOR 230V SDP-5 COVER "120V" MARKING OVER THE BAR CODE WITH "230V" LABEL (2 PLCS).
8. SLIP INNER BOX INTO OUTER SHIPPING BOX, CLOSE FLAPS AND TAPE.
9. PLACE SECOND ID LABEL ON OUTER SHIPPING BOX. FOR SDP-5 PLACE LABELS (S/N & P/N) IN BLANK SPACE NEAR PRINTED BAR CODE (4 PLCS). FOR 230V SDP-5 COVER "120V" MARKING OVER THE BAR CODE WITH "230V" LABEL (4 PLCS).

	SDP-5
	MC-8/B
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL
FINISH

ACAD 2002 FILE NAME: 15461-3

APPROVALS		DATE
DRAWN	AN	5/29/02
CHECKED	CLC	6/14/02
Q.C.	CW/DS	7/24/02
ISSUED	KB	7/31/02

lexicon

TITLE: ASSY DWG, SHIPMENT, MC-8/B, SDP-5

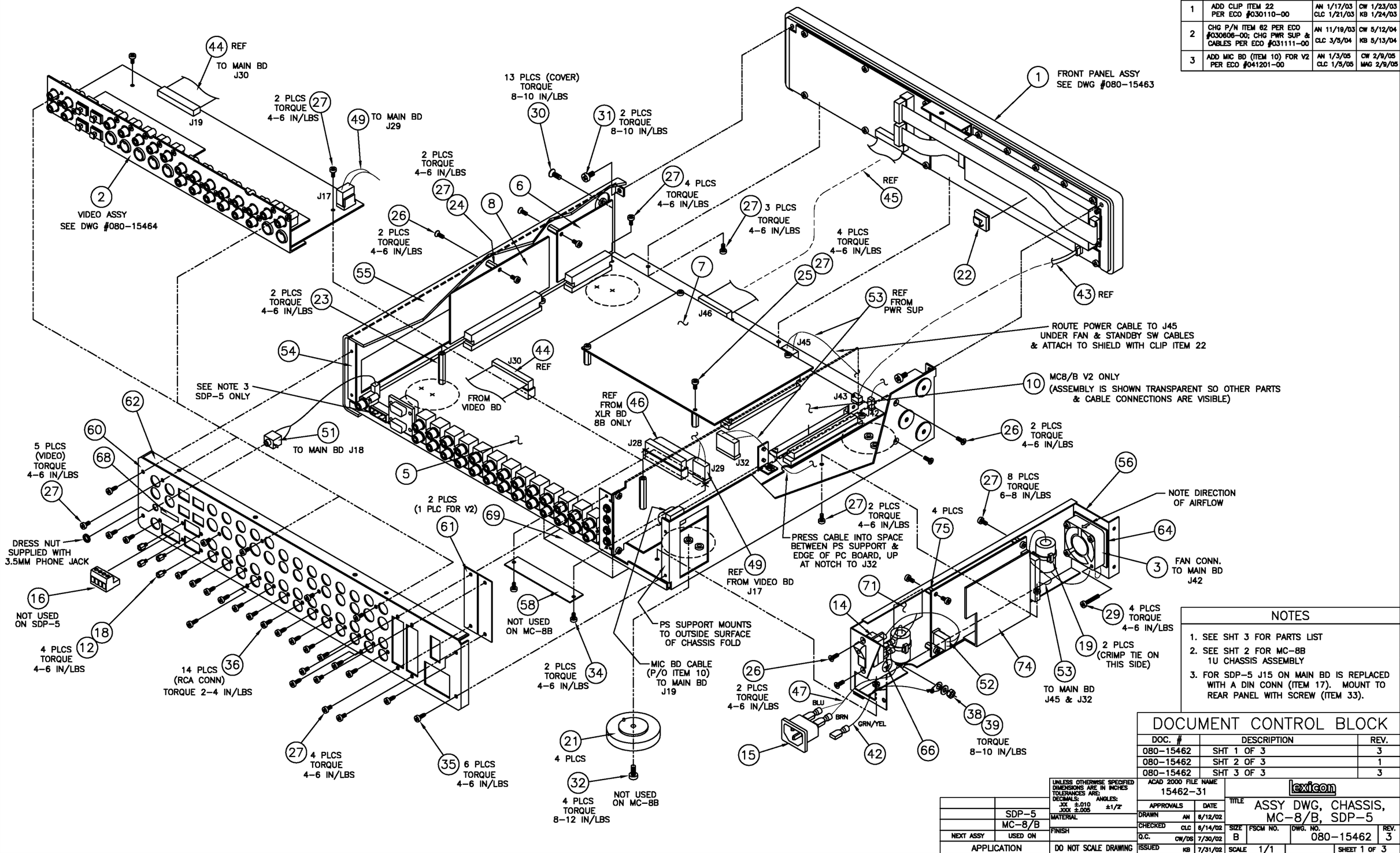
SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15461	3

SCALE 1/4 SHEET 1 OF 1

2/10/05

RELEASED COPY

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD CLIP ITEM 22 PER ECO #030110-00	AN 1/17/03 CLC 1/21/03	CW 1/23/03 KB 1/24/03
2	CHG P/N ITEM 62 PER ECO #030606-00; CHG PWR SUP & CABLES PER ECO #031111-00	AN 11/19/03 CLC 3/5/04	CW 5/12/04 KB 5/13/04
3	ADD MIC BD (ITEM 10) FOR V2 PER ECO #041201-00	AN 1/3/05 CLC 1/5/05	CW 2/9/05 MAG 2/9/05



NOTES

1. SEE SHT 3 FOR PARTS LIST
2. SEE SHT 2 FOR MC-8B 1U CHASSIS ASSEMBLY
3. FOR SDP-5 J15 ON MAIN BD IS REPLACED WITH A DIN CONN (ITEM 17). MOUNT TO REAR PANEL WITH SCREW (ITEM 33).

DOCUMENT CONTROL BLOCK

DOC. #	DESCRIPTION	REV.
080-15462	SHT 1 OF 3	3
080-15462	SHT 2 OF 3	1
080-15462	SHT 3 OF 3	3

	SDP-5
	MC-8/B
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH

ACAD 2000 FILE NAME: 15462-31

APPROVALS	DATE
DRAWN AN	6/12/02
CHECKED CLC	6/14/02
Q.C. CW/DS	7/30/02
ISSUED KB	7/31/02

lexicon

TITLE: ASSY DWG, CHASSIS, MC-8/B, SDP-5

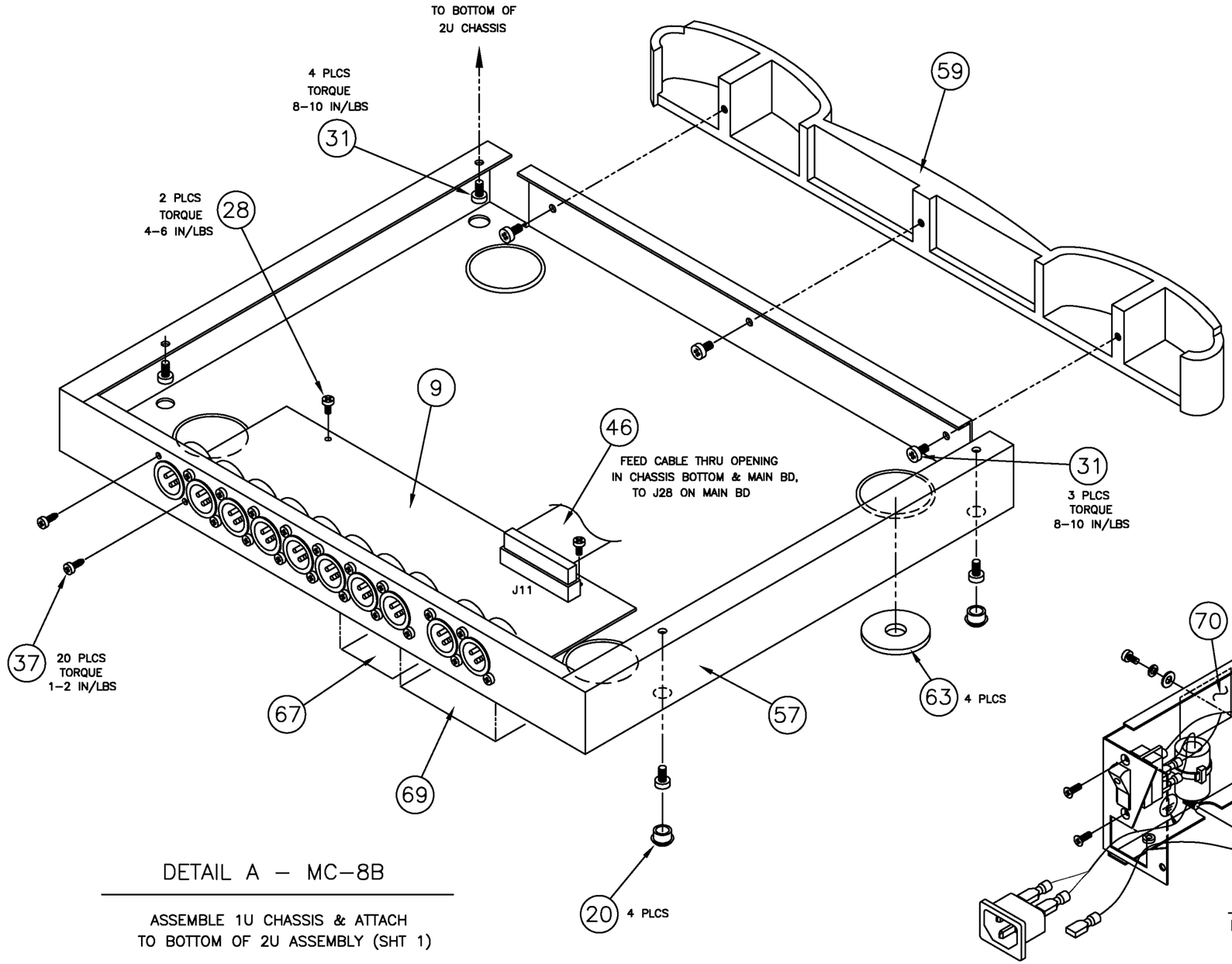
SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15462	3

SCALE 1/1 SHEET 1 OF 3

2/10/05

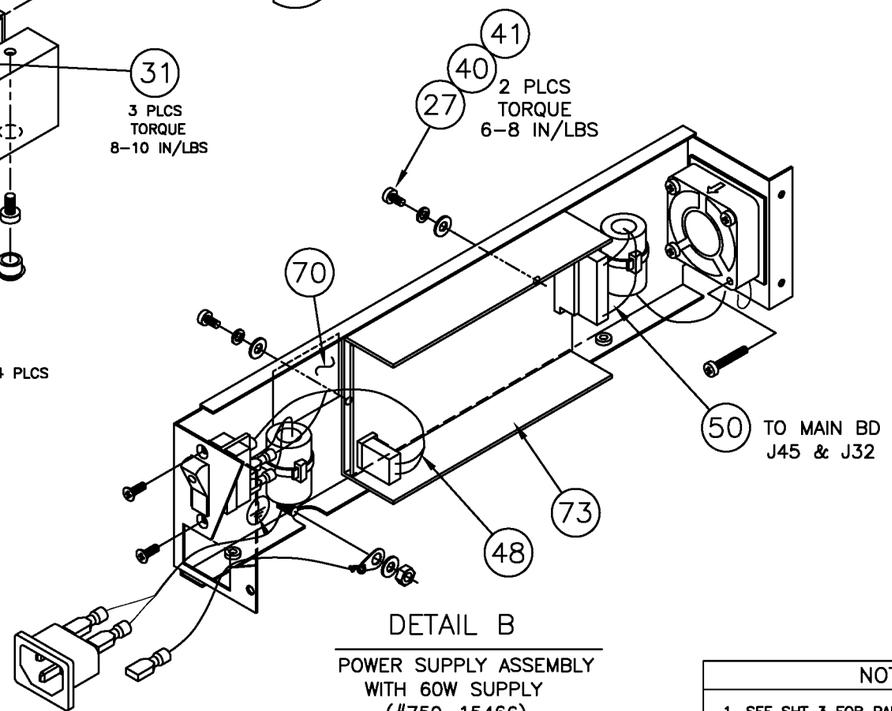
RELEASED COPY

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD DETAIL B – ITEM 73 PWR SUP PER ECO #031111-00	AN 11/18/03 CLC 3/5/04	CW 5/12/04 KB 5/13/04



DETAIL A – MC–8B

ASSEMBLE 1U CHASSIS & ATTACH
TO BOTTOM OF 2U ASSEMBLY (SHT 1)



DETAIL B

POWER SUPPLY ASSEMBLY
WITH 60W SUPPLY
(#750–15466)

NOTES

1. SEE SHT 3 FOR PARTS LIST
2. SEE SHT 1 FOR MC–8 (2U) ASSEMBLY

MC–8B	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15462–12

APPROVALS		DATE
DRAWN	AN	6/5/02
CHECKED	CLC	6/14/02
Q.C.	CW/DS	7/30/02
ISSUED	KB	7/30/02

lexicon

TITLE: ASSY DWG, CHASSIS, MC–8/B

SIZE	FSCM NO.	DWG. NO.	REV.
B		080–15462	1

SCALE 1/1 SHEET 2 OF 3

LEXICON, INC.

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
1.	022-15423	PL, MECH ASSY, FP, MC8/B	1	
	022-15756	PL, MECH ASSY, FP, SDP5		
2.	022-15426	PL, MECH ASSY, VIDEO	1	
3.	022-14850	PL, FAN ASSY	1	
4.				
5.	023-15428	PL, MAIN BD ASSY, MC8/B	1	
	023-15758	PL, MAIN BD ASSY, SDP5		
6.	023-15429	PL, MEMORY BD ASSY, MC8/B	1	
	023-15757	PL, MEMORY BD ASSY, SDP5		
7.	023-15434	PL, DSP BD ASSY	1	
8.	023-15436	PL, DECODER BD ASSY	1	
9.	023-15439	PL, XLR BD ASSY	1	(8B ONLY)
10.	023-16303	PL, MIC BD ASSY	1	(MC8/B V2 ONLY)
11.				
12.	120-09621	LOCTITE #242	–	D CONN JSCKT
13.				
14.	454-13850	SWITCH, ROCKER	1	
15.	490-11462	CONN, AC, 3C, SNAP, IEC	1	
16.	490-13144	CONN, PLUG, .200, 4FC, RA	1	(MC8, 8B)
17.	510-09790	CONN, DIN, 5FC@180DEG, PCRA, SHLD	1	MAIN BD J16 (SDP5 ONLY)
18.	527-12974	CONN, DSUB, JSCKT, 4-40	4	D CONN TO REAR PNL
19.	530-02488	TIE, CABLE, NYL	2	FERRITE SLV TO PS SPRT
20.	540-02472	PLUG, HOLE, 3/8", BLK	4	1U CHAS (8B ONLY)
21.	541-15458	FOOT, 1.97 DIA X .43H, ABS, BLK	4	CHASSIS (MC8, SDP5)
22.	530-09382	CLIP, WIRE HRNS, .15 DIA, ADH BAK	1	SHIELD
23.	635-13637	SPCR, M3X34MM, M/F, 6MM HEX	2	VIDEO TO MAIN BD
24.	635-14779	SPCR, M3X14MM, 6MM HEX	2	MEM & DECODER BDS TO CHASSIS
25.	635-15468	SPCR, M3X16MM, M/F, 6MM HEX	4	DSP BD TO MAIN BD
26.	640-10467	SCRW, M3X6MM, FH, PH	6	PS SPRT TO CHAS (2) MEM BD TO CHAS (1)
				DECD BD TO CHAS (1) PWR SW TO PS SPRT (2)
27.	640-10498	SCRW, M3X6MM, PNH, PH	34	VIDEO ASSY TO REAR PNL (5)
				VIDEO BD TO MAIN BD (2)
				MAIN BD TO CHASSIS (4)
				DSP BD TO MAIN BD (4)
				FRONT PANEL TO CHASSIS (3)
				PS SPRT TO CHASSIS (2)
				OPTION PANELS TO REAR (4)
				MEM & DECD BDS TO CHASSIS (2)
				PWR SUPPLY TO PS SPRT (8)
28.	640-10499	SCRW, M3X8MM, PNH, PH	2	XLR BD TO 1U CHASSIS (8B ONLY)
29.	640-12534	SCRW, M3X20MM, PNH, PH	4	FAN TO PS SPRT
30.	640-13645	SCRW, M4X10MM, FH, SCKT	13	COVER TO CHASSIS
31.	640-15476	SCRW, M4X8MM, PNH, PH	9	FP TO CHAS (2), 1U CHAS TO 2U CHAS (4, 8B)
				1U FRT TO 1U CHAS (3, 8B)
32.	640-15477	SCRW, M4X12MM, PNH, PH	4	FEET TO CHAS (MC8, SDP5)
33.	641-12759	SCRW, TAP, AB, #2X1/4, PNH, PH, BZ	1	DIN CONN TO REAR PNL (SDP5 ONLY)
34.	641-01703	SCRW, TAP, AB, #4X1/4, PNH, PH	2	ACCESS PNL TO CHASSIS BOTTOM (MC8, SDP5)
35.	641-10989	SCRW, TAP, AB, #4X3/8, PNH, PH	6	REAR PNL TO CHASSIS
36.	641-11466	SCRW, TAP, #4X3/8, PNH, PH, TRI	14	RCA CONN TO REAR PNL
37.	641-14898	SCRW, TAP, #4X1/4, PNH, PH, BZ, TRI	20	XLR CONN TO 1U CHASSIS (8B ONLY)
38.	643-10492	NUT, M4X.7MM, KEP	1	CHASSIS GND
39.	644-10494	WSHR, FL, M4 CL X 9 OD X .8MM THK	1	CHASSIS GND
40.	644-01737	WSHR, LOCK, SPLIT, #4	2	PWR SUPPLY TO PS SPRT (60W PS ONLY)
41.	644-02716	WSHR, FL, #4CL X .312 OD X .03 THK	2	PWR SUPPLY TO PS SPRT (60W PS ONLY)
42.	680-11461	WIRE, 18G, G/Y, 2.5", .187 QDC/LUG #8	1	AC CONN TO CHASSIS GND
43.	680-14854	CABLE, .079, SCKT/SCKT, 4C, 4"	REF	STANDBY BD TO MAIN BD
44.	680-15469	CABLE, .100, PLUG/SCKT, 2X17C, 2"L	REF	VIDEO BD TO MAIN BD
45.	680-14083	CABLE, .100, PLUG/SCKT, 2X13C, 2"L	REF	SW/LED BD TO MAIN BD
46.	680-14494	CABLE, .100, SCKTX2-180, 2X17C, 6"L	1	MAIN BD TO XLR BD (8B ONLY)
47.	680-14536	CABLE, PWR, .187/.110 QDC, SLV, 4.5"	1	AC CONN TO PWR SW
48.	680-14537	CABLE, PWR, HSG/.110 QDC, 2C, 5"	1	PWR SW TO 60W PWR SUP
49.	680-14539	CABLE, HSG/HSG, 4C, 4"	1	MAIN BD TO VIDEO BD
50.	680-15465	CABLE, HSG/HSG, 8C, SLV, 16/17	1	60W PWR SUP TO MAIN BD
51.	680-15470	CABLE, 3.5MM JACK/HSG, 2C, 3"	1	IR CONN TO MAIN BD
52.	680-16405	CABLE, PWR, HSG/.110 QDC, 2C, 5" P3=N	1	PWR SW TO 80W PWR SUP
53.	680-16406	CABLE, HSG/HSG, 12/10C, SLV, 16/17	1	80W PWR SUP TO MAIN BD
54.	700-15447	CHASSIS, 2U	1	
55.	700-15448	COVER, 2U	1	
56.	700-15449	SUPPORT, PS	1	
57.	700-15450	CHASSIS, IU	1	8B ONLY
58.	702-14495	PANEL, ACCESS	1	CHASSIS BOTTOM (MC8, SDP5)
59.	702-14454	PANEL, FRONT, 1U	1	8B ONLY
60.	702-15444	PANEL, REAR, MC8/B	1	
	702-15766	PANEL, REAR, SDP5		
61.	702-15457	PANEL, OPTION, BLANK	2	REAR PANEL (QTY 1 FOR MC8/B V2)
62.	720-15656	TAPE, CU, EMBOSSED, PSA, 16.7 X .5"	1	TOP FOLD OF REAR PANEL
63.	720-13632	PAD, FOOT	4	1U CHASSIS BOTTOM (8B ONLY)
64.	720-14852	GASKET, FAN	1	FAN TO PS SUPPORT
65.				
66.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	PS SUPPORT
67.				
68.	740-09538	LABEL, S/N, CHASSIS	1	REAR PANEL
69.	740-14888	LABEL, LIC/PAT/WARN	1	CHASSIS BOTTOM
70.	740-15745	LABEL, FUSE, CAUTION – (60W PS)	1	PS SUPPORT
71.	740-16403	LABEL, FUSE, CAUT – (80W PS)		
72.				
73.	750-15466	PWR SUP, +-5V/+-15V, 60W	1	(SEE BOM & SHT 2 DETAIL B FOR 60W PS)
74.	750-16408	PWR SUP, +-5V/+-15V, 80W		
75.	635-12112	SPCR, M3X10MM,6MM HEX	4	80W PS TO PS SPRT

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD CLIP ITEM 22 PER ECO #030110-00	AN 1/17/03 CLC 1/21/03	CW 1/23/03 KB 1/24/03
2	CHG P/N ITEM 62 PER ECO #030806-00; CHG PWR SUP & CABLES PER ECO #031111-00	AN 3/2/04 CLC 3/5/04	CW 5/12/04 KB 5/13/04
3	ADD ITEM 10 FOR MC8/B V2, CHG 61 PER ECO #041201-00	AN 1/3/05 CLC 1/5/05	CW 2/9/05 MAG 2/9/05

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOMS.

	SDP-5
	MC-8/B
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15462-33

APPROVALS	DATE
DRAWN AN	8/12/02
CHECKED CLC	8/14/02
Q.C. CW/DS	7/30/02
ISSUED KB	7/31/02

lexicon

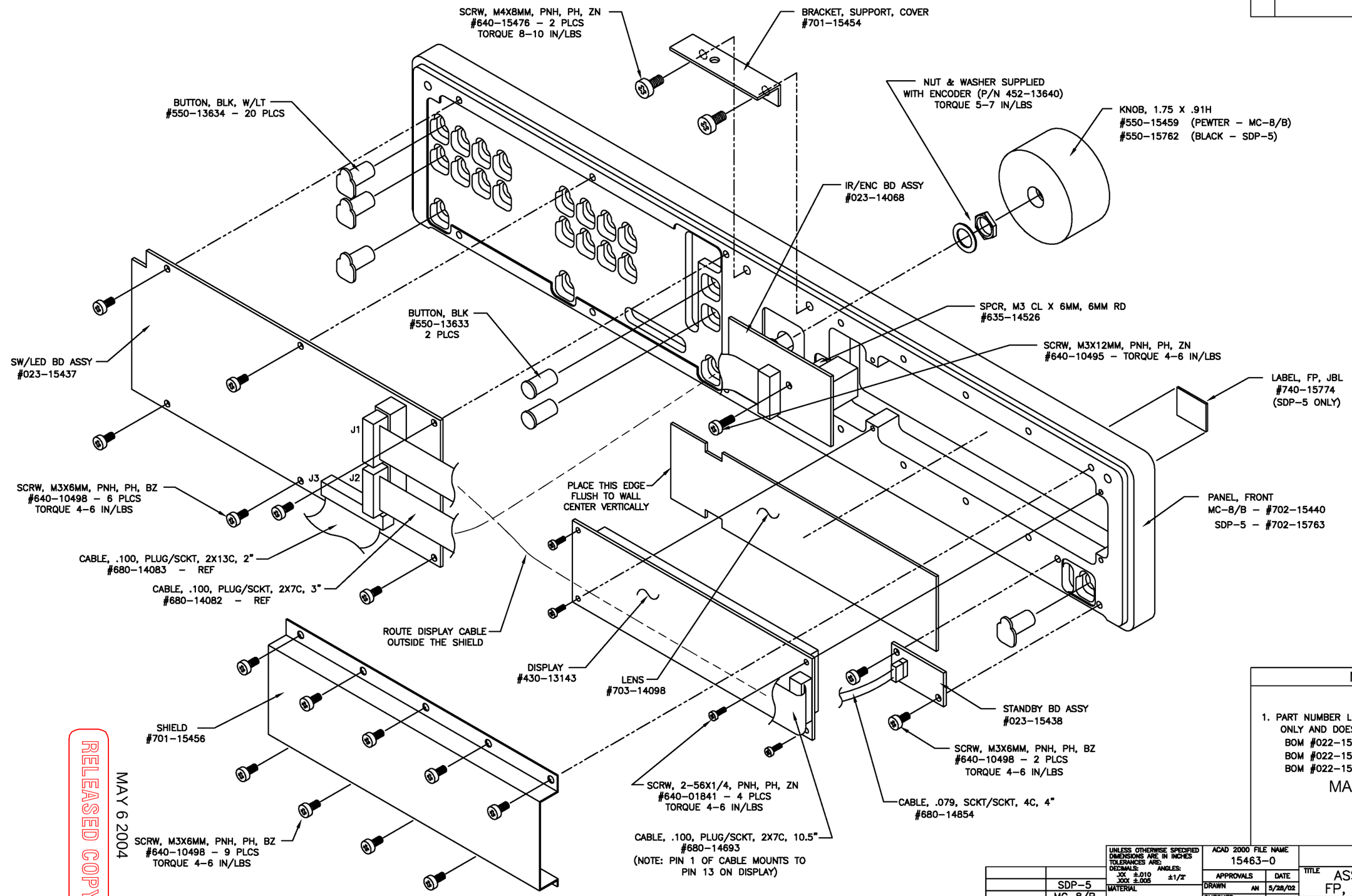
TITLE: ASSY DWG, CHASSIS MC-8/B, SDP-5

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15462	3

SCALE: NONE SHEET 3 OF 3

LEXICON, INC.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH



RELEASED COPY

MAY 6 2004

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE
   BOM #022-15424 COMMON
   BOM #022-15423 MC-8/B
   BOM #022-15756 SDP-5

MAY 6 2004

	SDP-5
	MC-8/B
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15463-0

APPROVALS		DATE
DRAWN	AN	5/28/02
CHECKED	CLC	5/14/02
Q.C.	CW/DS	7/24/02
ISSUED	KB	7/31/02

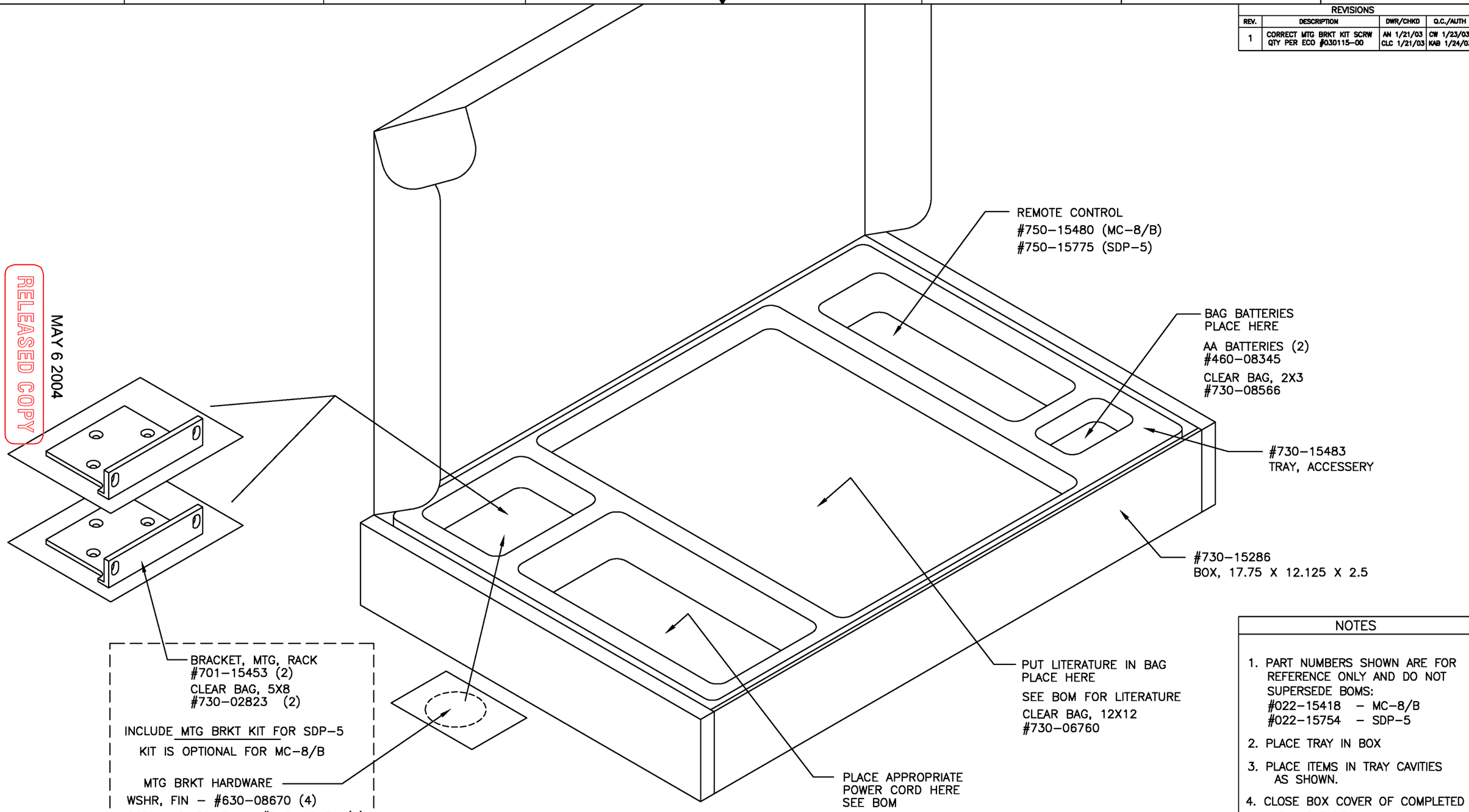
Lexicon

TITLE: ASSY DWG, MECH, FP, MC-8/B, SDP-5

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-15463	0

SCALE 1/2 SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CORRECT MTG BRKT KIT SCRW QTY PER ECO #030115–00	AN 1/21/03 CLC 1/21/03	CW 1/23/03 KAB 1/24/03



NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOMS:
   #022–15418 – MC–8/B
   #022–15754 – SDP–5
2. PLACE TRAY IN BOX
3. PLACE ITEMS IN TRAY CAVITIES AS SHOWN.
4. CLOSE BOX COVER OF COMPLETED KIT AND TAPE.

MAY 6 2004

	SDP–5
	MC–8/B
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME: 15482–1

APPROVALS		DATE
DRAWN	AN	9/30/02
CHECKED	CLC	10/7/02
Q.C.	CW	10/7/02
ISSUED	KB	10/10/02

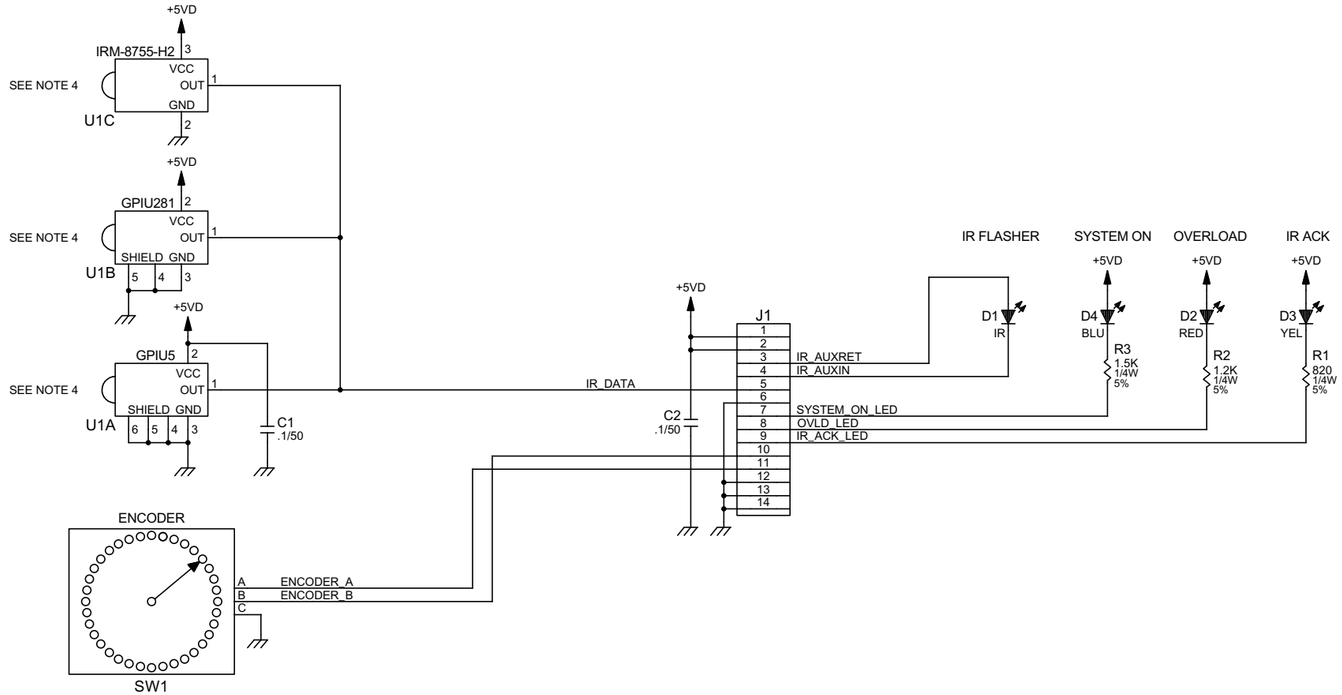
lexicon

TITLE: ASSY DWG, ACCESS, MC–8/B, SDP–5

SIZE	FSCM NO.	DWG. NO.	REV.
B		080–15482	1

SCALE 1/2 SHEET 1 OF 1

LEXICON, INC.



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 000327-00	RWH 3/27/00	CW 4/28/00
		KB 4/10/00	KB 4/10/00
2	CHANGED PER DCR 000925-01	RWH 10/13/00	CW 10/23/00
		KB 10/20/00	KB 10/20/00
3	CHANGED R3 FROM 2.4K TO 1.5K PER ECO 010130-00	CW 1/30/01	ECM 1/30/01
		KB 1/30/01	KB 1/30/01

NOTES

1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

2 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

3 LAST REFERENCE DESIGNATORS USED: C2, D4, J1, R3, SW1, U1

4 INSTALL ONE ONLY OF U1A, B, C.

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	CW	10/27/99
CHECKED	KB	10/27/99
Q.C.	RWH	10/27/99
ISSUED	KB	10/27/99

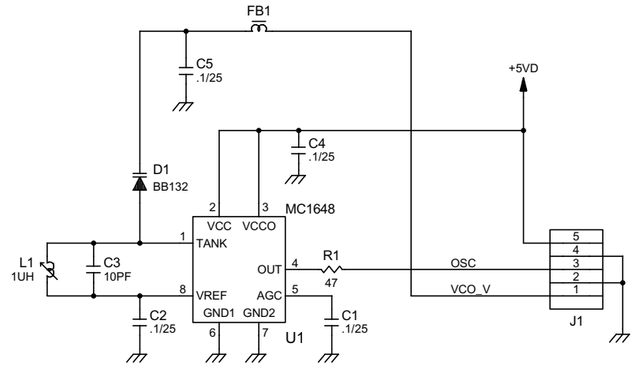
TITLE: SCHEM,IR/ENC BD,MC12

SIZE	CODE	NUMBER	REV
B		060-13699	3

FILE NAME: 13699-3.1

SHEET 1 OF 1

1-30-2001_15:17



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C5, D1, FB1, J1, L1, R1, U1.

REFERENCE COPY

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	10/25/00
CHECKED	ECM	11/7/00
Q.C.	CW	11/7/00
ISSUED	KB	11/7/00

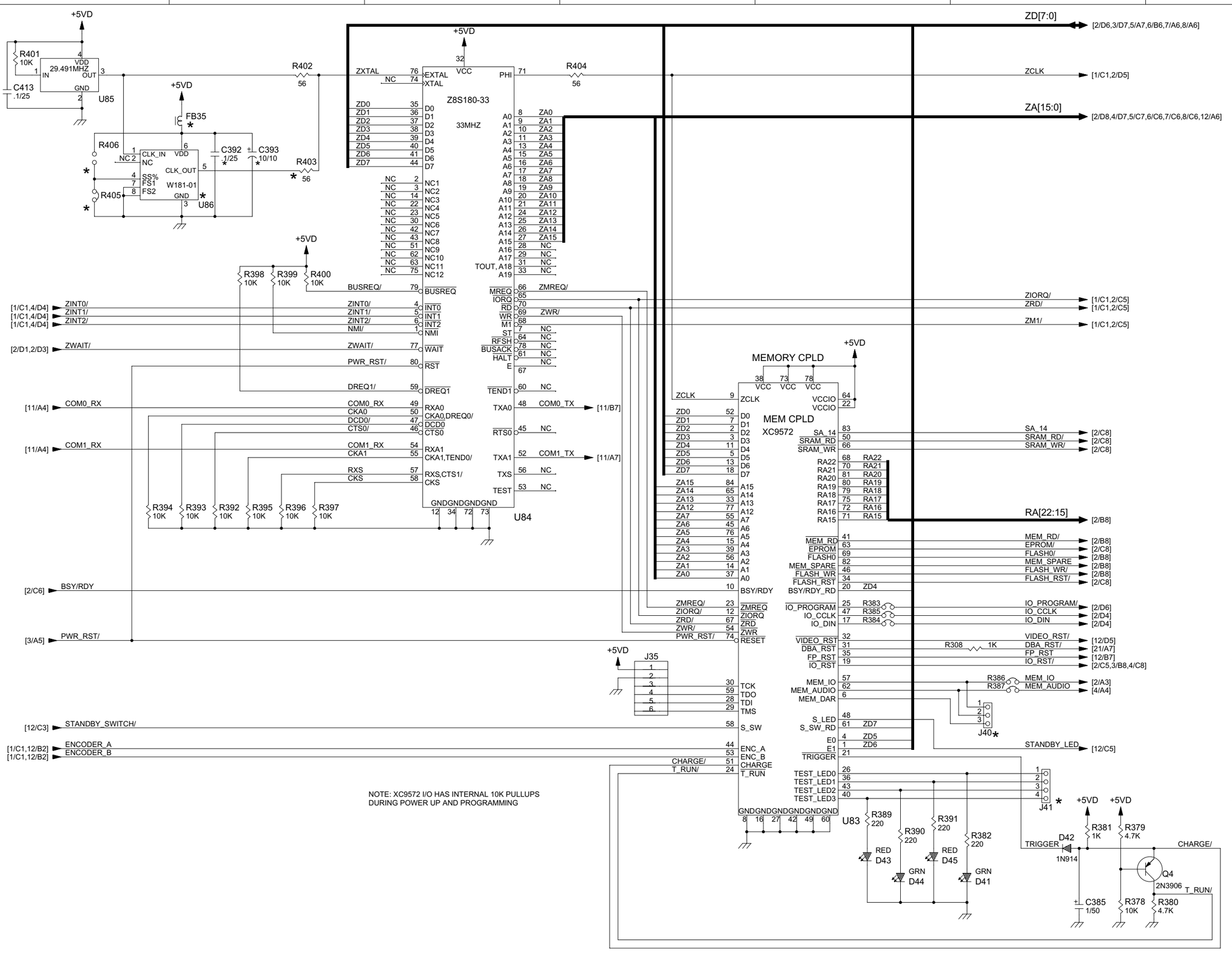
TITLE: SCHEM, VCO BD, MC12

SIZE	CODE	NUMBER	REV
B		060-14849	0

FILE NAME: 14849-0.1

SHEET 1 OF 1

11-8-2000_9:31



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	CHANGED SHEETS 10, 13, 14 PER ECO 030213-00	RWH 02/19/03	CW 02/20/03
		CBV 02/19/03	KB 02/20/03
5	CHANGED SHEET 22 PER ECO 031111-00	RWH 3/2/04	CW 5/25/04
		GAP 5/18/04	KAB 5/26/04
6	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

OCT 27 2004 RELEASED COPY

TEST POINTS

ZCLK ZMREQ/ ZIORQ/ ZRD/ ZWR/ ZM1/
ENC_A ENC_B
ZINT0/ ZINT1/ ZINT2/

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: BAT1, C415, D61, E34, FB35, J48, L1, Q9, R440, RY5, U98, W3.

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

8 COMPONENTS MARKED WITH § ARE NOT INSTALLED ON MC4.

DOCUMENT CONTROL BLOCK: #060-15259

SHEET	REVISION	TITLE
1 OF 23	6	HOST & MEMORY CPLD
2 OF 23	4	MEMORY CONN, RAM, I/O CPLD
3 OF 23	4	STATUS & CTL REGISTERS, IR RCVR
4 OF 23	4	AUDIO FPGA
5 OF 23	4	DSP BOARD CONNECTOR
6 OF 23	4	OPTION BD 0 CONNECTOR
7 OF 23	4	OPTION BD 1 CONNECTOR
8 OF 23	4	OPTION BD 2 CONNECTOR
9 OF 23	4	DIGITAL AUDIO RECEIVERS & ZONE DIGITAL OUTPUT
10 OF 23	5	PHASE LOCK LOOP
11 OF 23	4	REMOTE POWER & RS232 PORTS
12 OF 23	4	FRONT PANEL,STANDBY,VIDEO CONN
13 OF 23	5	LEFT ANALOG INPUT MUXES
14 OF 23	5	RIGHT ANALOG INPUT MUXES
15 OF 23	4	MIC INPUTS & MAIN A/D CONVERTER
16 OF 23	4	ZONE2 DAC
17 OF 23	4	L/R FRONT DACS
18 OF 23	4	CENTER/SUB DACS
19 OF 23	4	L/R SIDE DACS
20 OF 23	4	L/R REAR DACS
21 OF 23	4	XLR BD CONN,CONTROL REG
22 OF 23	5	POWER SUPPLY
23 OF 23	4	BYPASS CAPACITORS

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

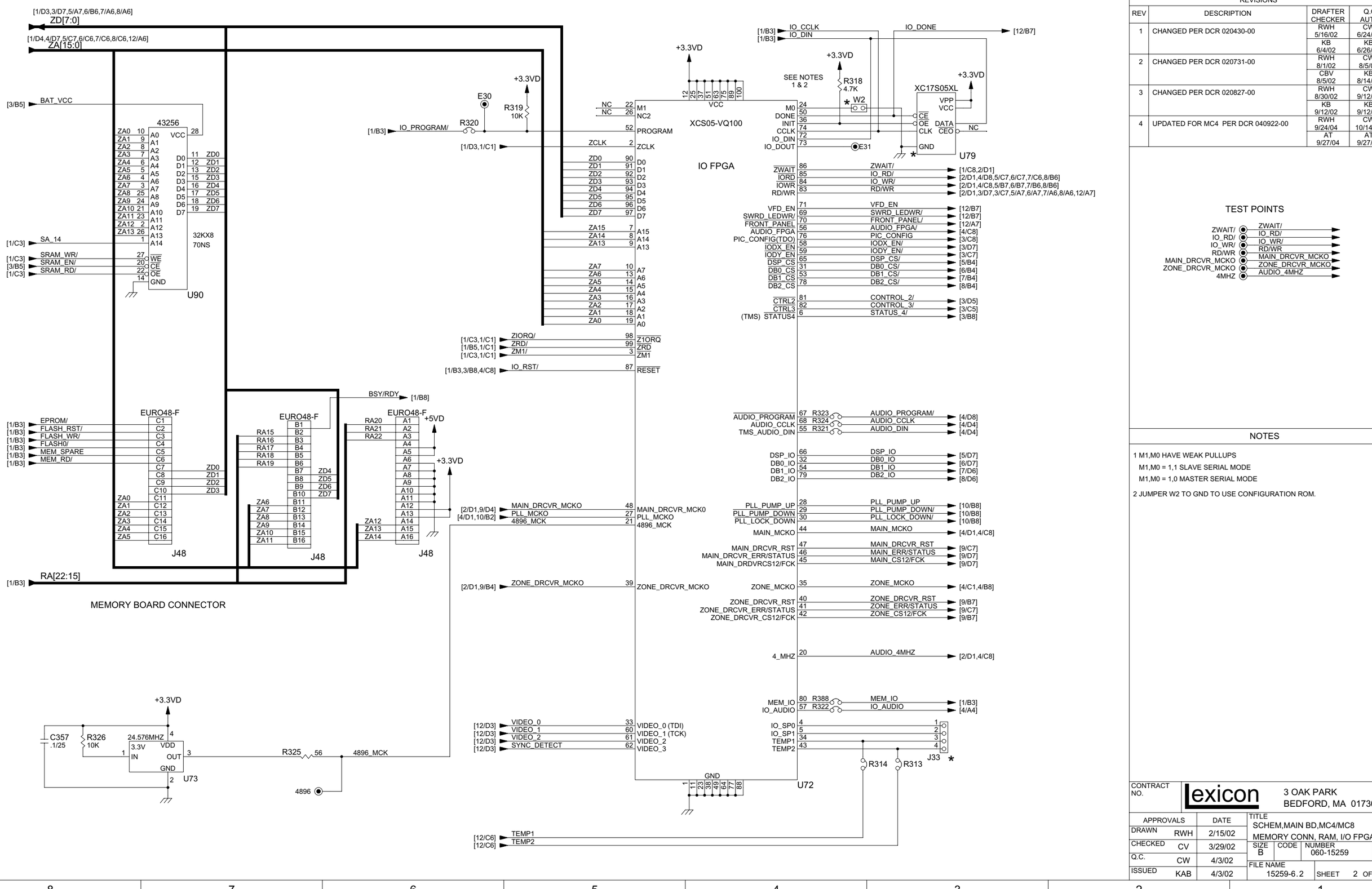
APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE
SCHEM,MAIN BD,MC4/MC8
HOST & MEMORY CPLD

SIZE	CODE	NUMBER	REV
B		060-15259	6

FILE NAME 15259-6.1 SHEET 1 OF 23

10-19-2004 8:58



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

TEST POINTS

ZWAIT/ IO_RD/ IO_WR/ RD/WR MAIN_DRCVR_MCKO ZONE_DRCVR_MCKO 4MHZ

AUDIO_4MHZ

NOTES

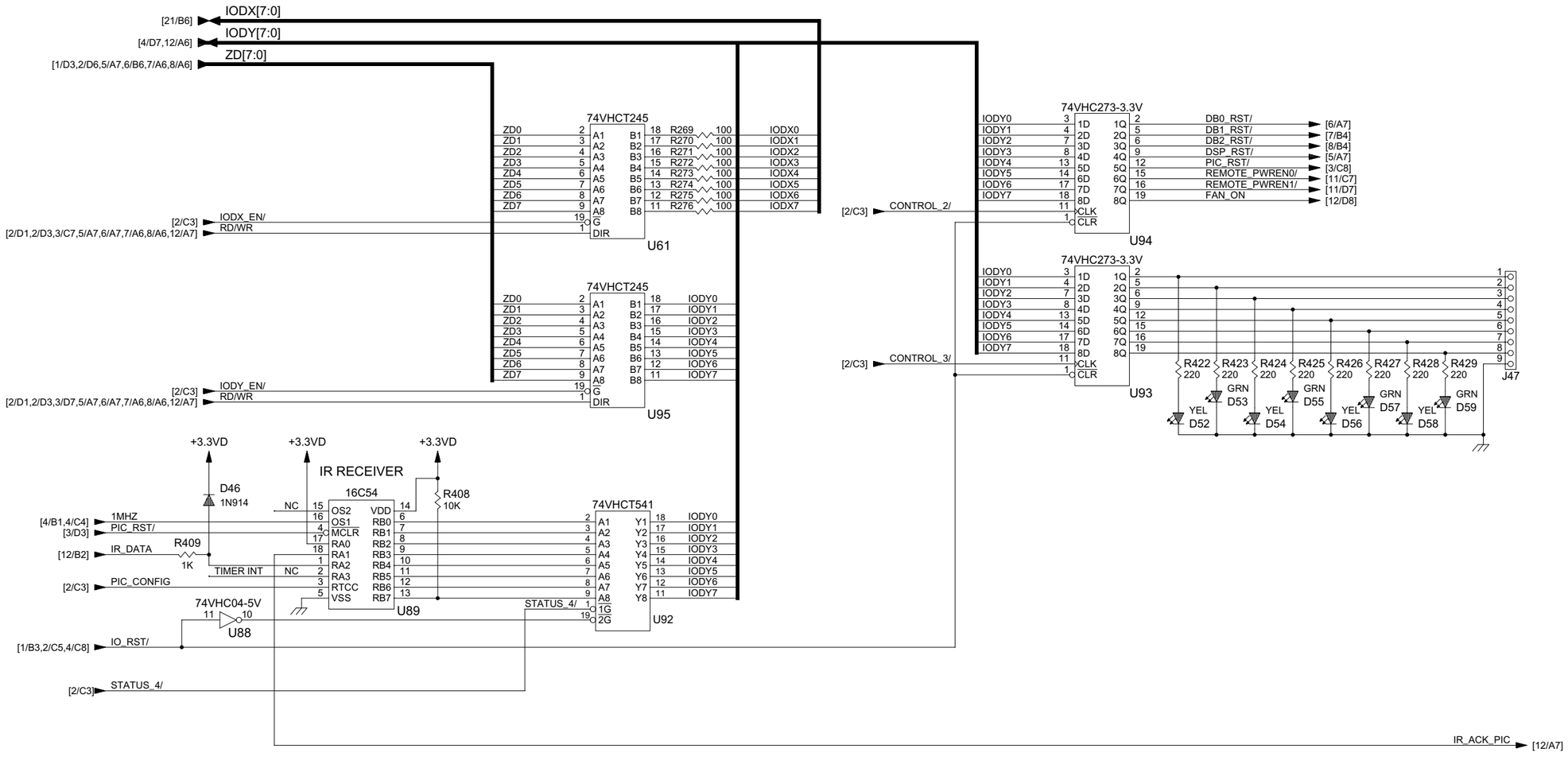
1 M1,M0 HAVE WEAK PULLUPS
M1,M0 = 1,1 SLAVE SERIAL MODE
M1,M0 = 1,0 MASTER SERIAL MODE

2 JUMPER W2 TO GND TO USE CONFIGURATION ROM.

CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 MEMORY CONN, RAM, I/O FPGA
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B | CODE | NUMBER 060-15259 | REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.2 | SHEET 2 OF 23

10-19-2004_8:58

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

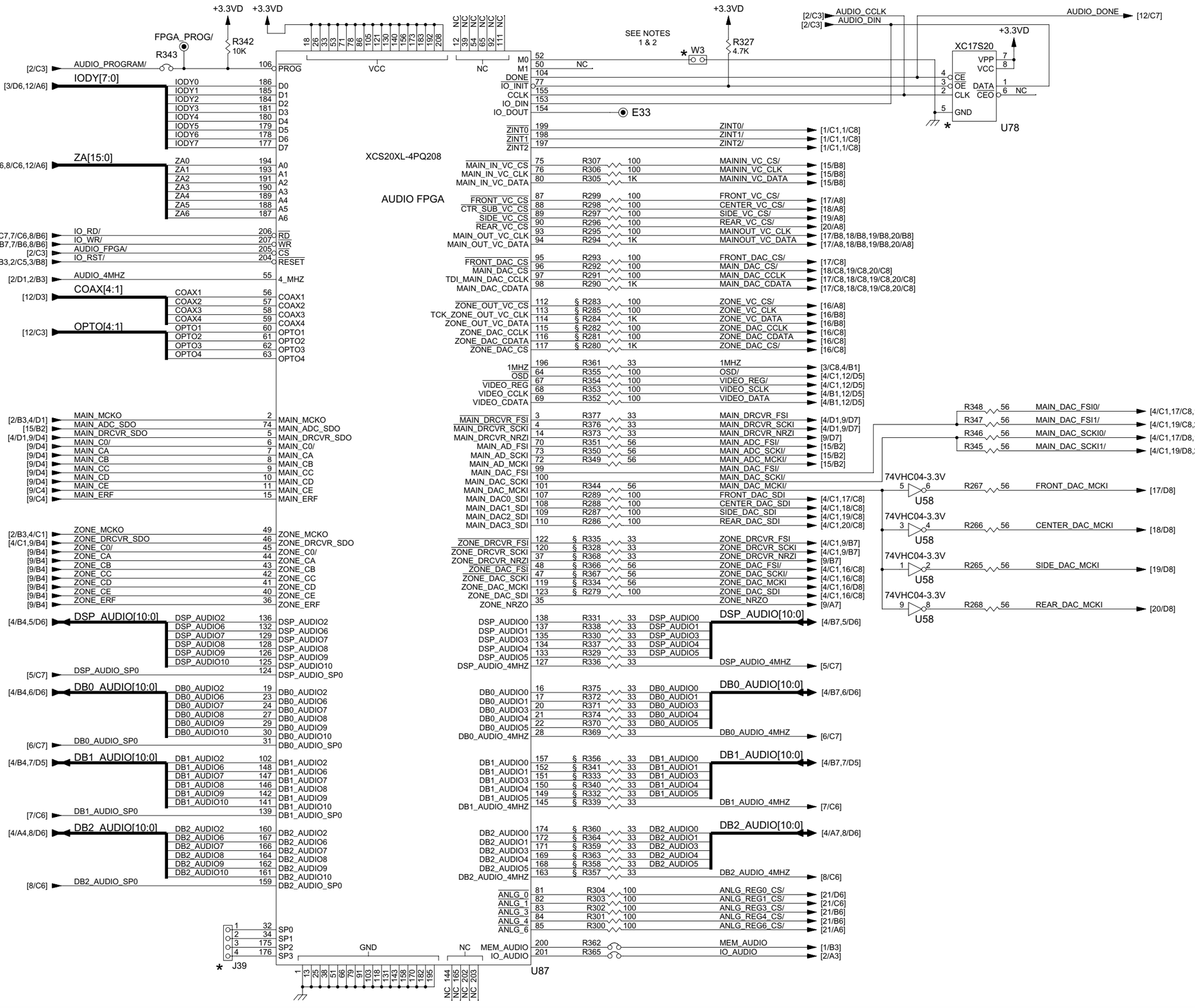
TITLE
SCHEM,MAIN BD,MC4/MC8
STATUS & CTL REGISTERS, IR RCVR

SIZE	CODE	NUMBER	REV
B		060-15259	4

FILE NAME 15259-6.3

SHEET 3 OF 23

10-19-2004 8:58



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

TEST POINTS MAIN PATH

PLL_OUT — PLL_MCKO
MMCK — MAIN_MCKO

MDRX_FSI — MAIN_DRCVR_FSI
MDRX_SCKI — MAIN_DRCVR_SCKI
MDRX_SDO — MAIN_DRCVR_SDO

MDAC_FSI — MAIN_DAC_FSI/
MDAC_FCKI — MAIN_DAC_SCKI/
MDAC_MCKI — MAIN_DAC_MCKI/
FDAC_SDI — FRONT_DAC_SDI
CDAC_SDI — CENTER_DAC_SDI
SDAC_SDI — SIDE_DAC_SDI
RDAC_SDI — REAR_DAC_SDI

MDAC_FSI0 — MAIN_DAC_FSI0/
MDAC_FSI1 — MAIN_DAC_FSI1/
MDAC_SCKI0 — MAIN_DAC_SCKI0/
MDAC_SCKI1 — MAIN_DAC_SCKI1/

ZONE PATH

ZMCK — ZONE_MCKO
ZDRX_FSI — ZONE_DRCVR_FSI
ZDRX_SCKI — ZONE_DRCVR_SCKI
ZDRX_SDO — ZONE_DRCVR_SDO

ZDAC_FSI — ZONE_DAC_FSI/
ZDAC_SCKI — ZONE_DAC_SCKI/
ZDAC_MCKI — ZONE_DAC_MCKI
ZDAC_SDI — ZONE_DAC_SDI

VIDEO CONTROL

OSD — OSD/
VREG — VIDEO_REG/
VSCLK — VIDEO_SCLK
VDATA — VIDEO_DATA

PIC CLOCK

1MHZ — 1MHZ

SPARES

+3.3VD
74VHC04-3.3V U58 (11 → 10 NC)
74VHC04-3.3V U58 (13 → 12 NC)

NOTES

1 M1,M0 HAVE WEAK PULLUPS
M1,M0 = 1,1 SLAVE SERIAL MODE
M1,M0 = 1,0 MASTER SERIAL MODE

2 JUMPER W3 TO GND TO USE CONFIGURATION ROM.

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE	SCHEM,MAIN BD,MC4/MC8 AUDIO FPGA
DRAWN RWH	2/15/02		
CHECKED CV	3/29/02	SIZE B / CODE / NUMBER 060-15259 / REV 4	
Q.C. CW	4/3/02		
ISSUED KAB	4/3/02	FILE NAME 15259-6.4 / SHEET 4 OF 23	

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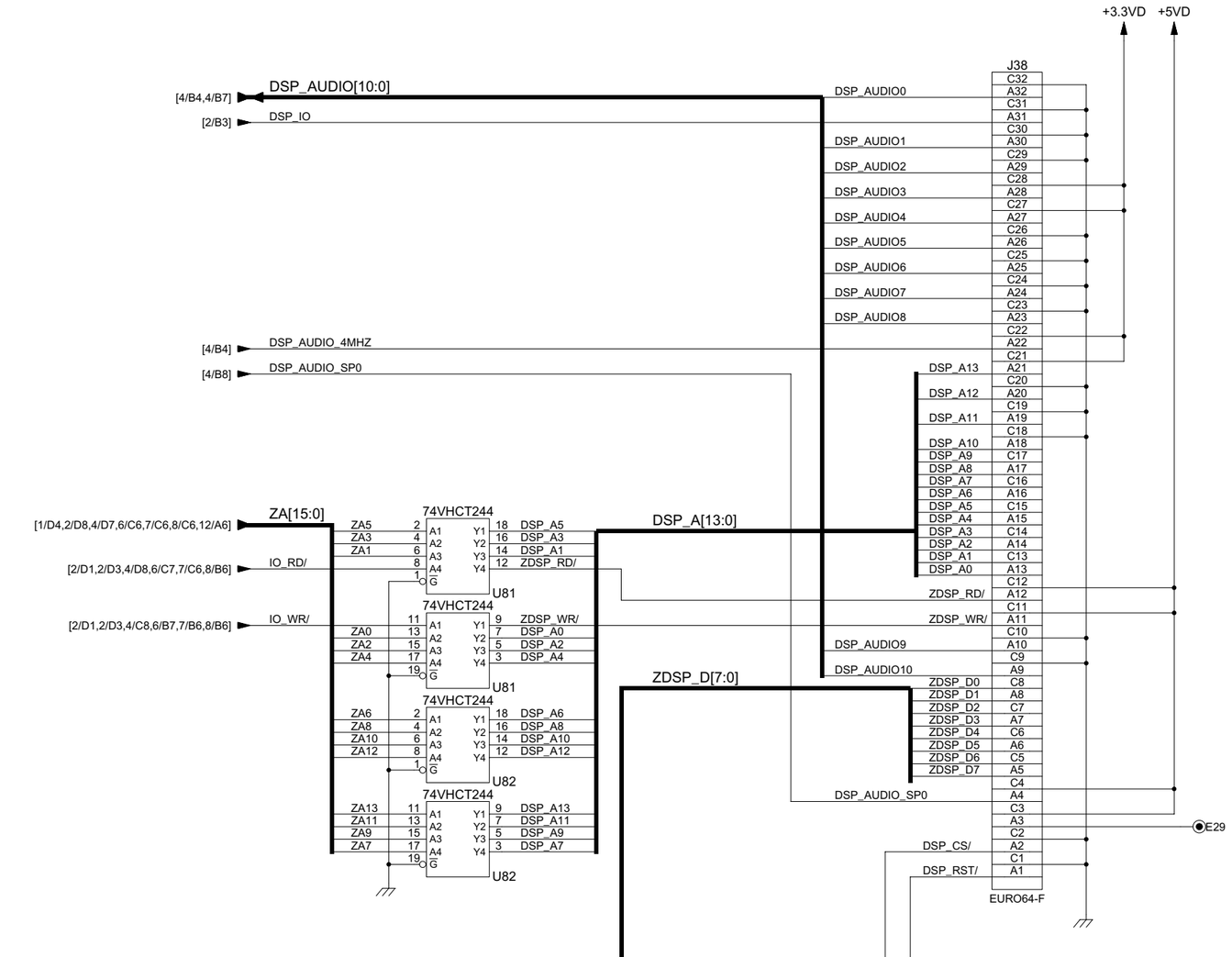
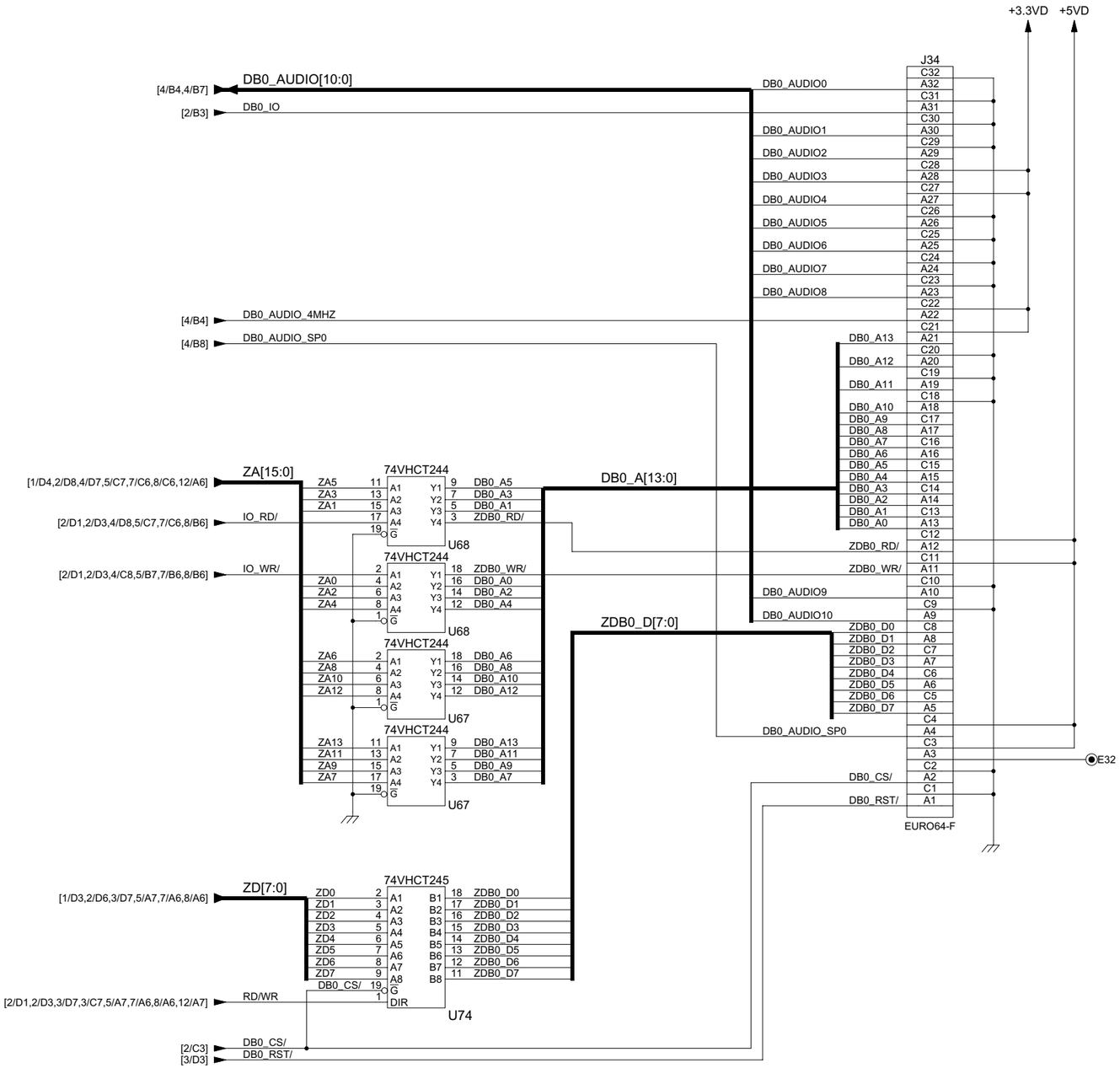
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN RWH	2/15/02	SCHEM,MAIN BD,MC4/MC8 DSP BOARD CONNECTOR	
CHECKED CV	3/29/02	SIZE B / CODE / NUMBER 060-15259	REV 4
Q.C. CW	4/3/02	FILE NAME 15259-6.5	SHEET 5 OF 23
ISSUED KAB	4/3/02		

10-19-2004_8:58

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 OPTION BD 0 CONNECTOR
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B / CODE / NUMBER 060-15259 / REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.6 / SHEET 6 OF 23

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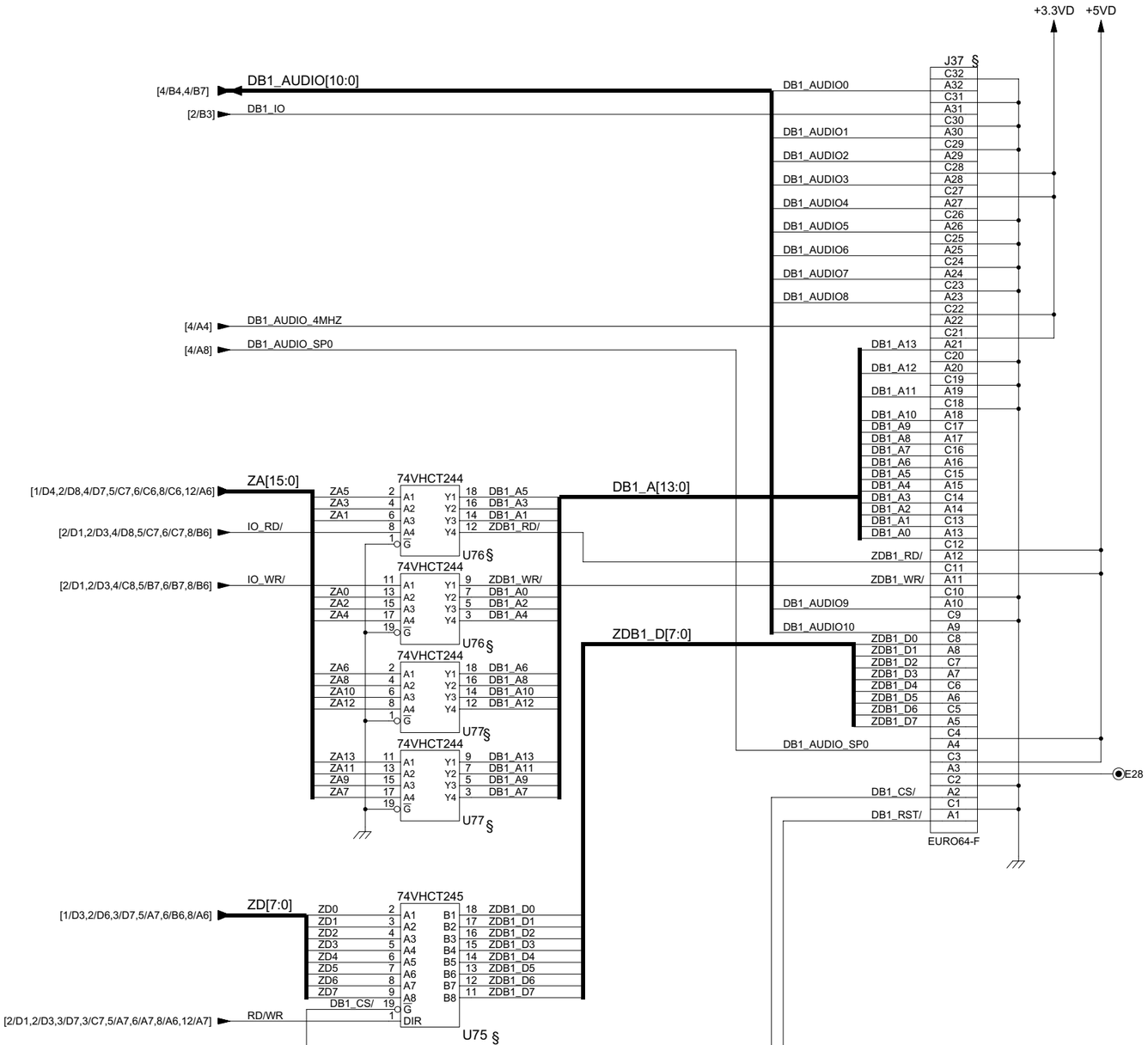

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 COMPONENTS ON THIS PAGE ARE NOT INSTALLED ON MC4

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE: SCHEM,MAIN BD,MC4/MC8 OPTION BD 1 CONNECTOR

SIZE	CODE	NUMBER	REV
B		060-15259	4

FILE NAME: 15259-6.7 SHEET 7 OF 23

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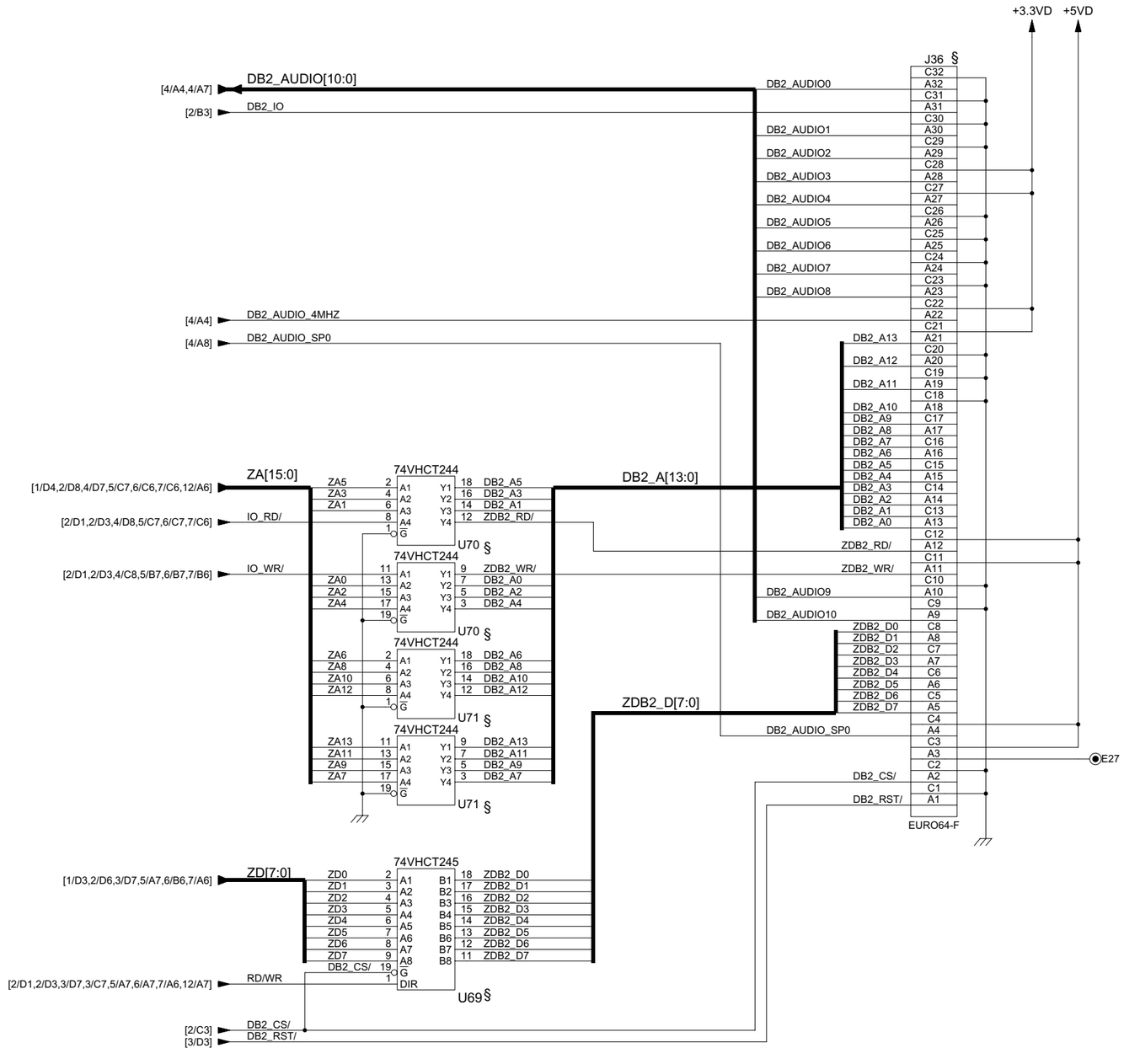

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 COMPONENTS ON THIS PAGE ARE NOT INSTALLED ON MC4

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 OPTION BD 2 CONNECTOR
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B | CODE | NUMBER 060-15259 | REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.8 | SHEET 8 OF 23

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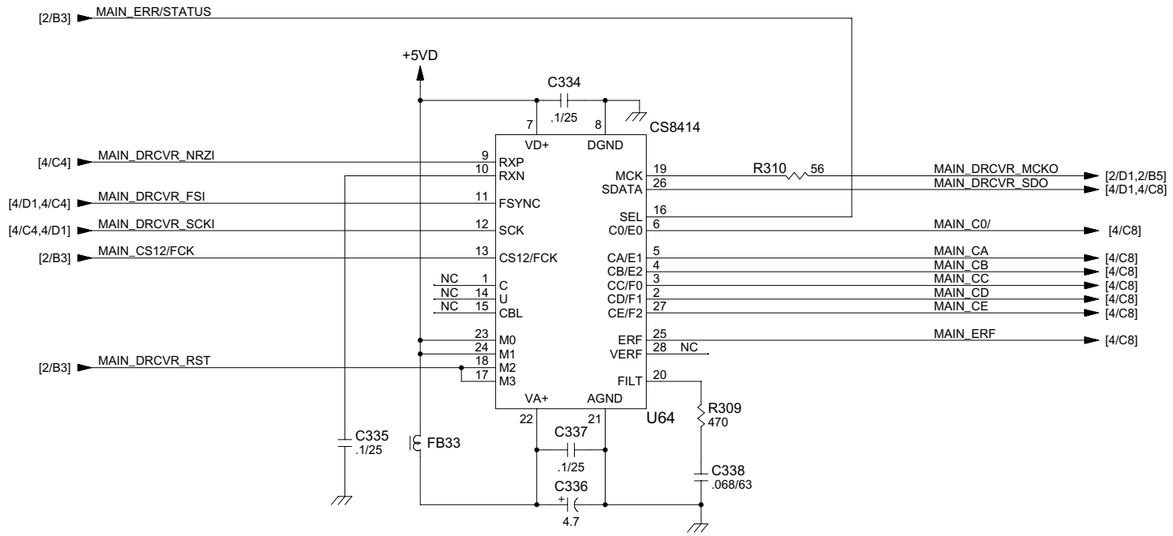
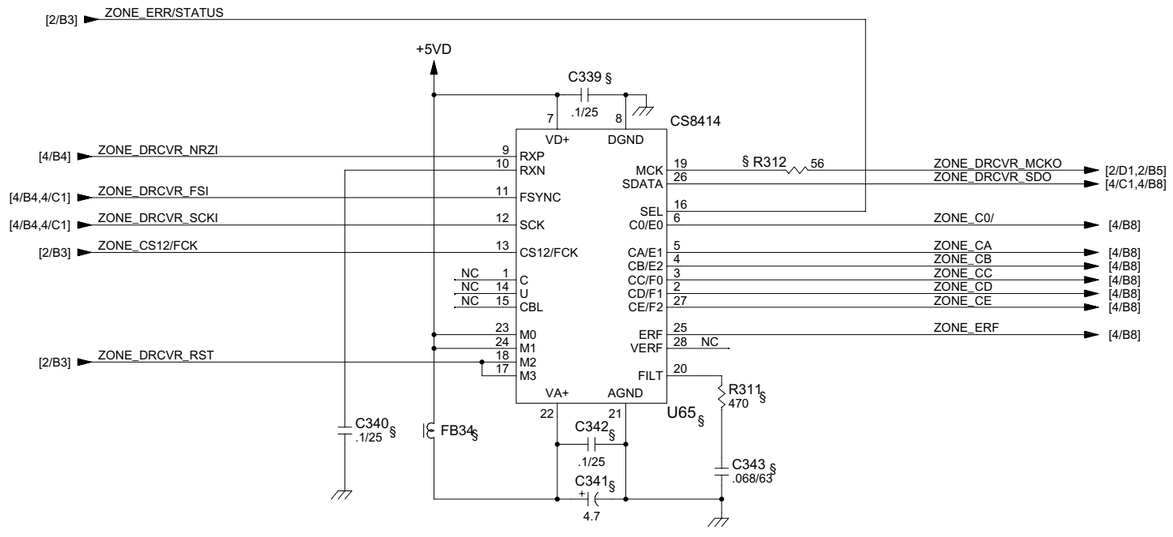
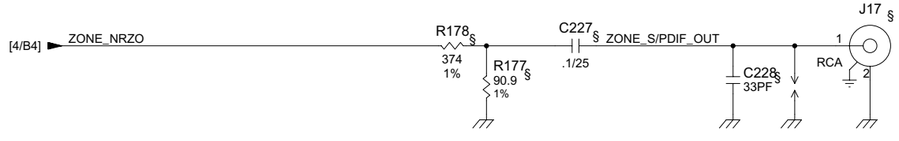
MAIN DIGITAL AUDIO RECEIVER



ZONE DIGITAL AUDIO RECEIVER



ZONE DIGITAL OUTPUT



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE
SCHEM,MAIN BD,MC4/MC8
DIGITAL AUDIO RECEIVERS AND
ZONE DIGITAL OUTPUT

SIZE	CODE	NUMBER	REV
B		060-15259	4

FILE NAME 15259-6.9
SHEET 9 OF 23

10-19-2004_9:02

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	CHANGED U56 PER ECO 030213-00	RWH 02/19/03	CW 02/20/03
		CBV 02/19/03	KB 02/20/03
5	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

+15V
+5VD
78L05
VIN
VOUT
COMMON
U54
1N4002
D27
D26
1N4002
C292
.1/25
C293
10/10
+5_PLL
+5_PLCC
FB25
C294
.1/25
FB28
C307
.1/25
FB26
C297
.1/25
D33
1N914
C302
1/50
R261
1.2K
C303
47/16
+15V
LF353
U56
-15V
VCOV
R264
100
C304
.1/25
VCOV
J31
VCO MODULE
VCO
OSC
C296
.1/25
74HCU04
U57
R259
47K
R258
47K
C295
.1/25
R260
56
PLL_MCKO
[2/B5,4/D1]
44.1K AND 48K @ 512FS
88.2K AND 96K @ 256 FS
[2/B3]
PLL_PUMP_UP
U55
74ACT04
UP/
D30
BAR35
R255
1.2K
P_UP/
PLL_PUMP_DOWN/
P_DOWN
D31
R256
1.2K
P_DN
PLL_LOCK_DOWN/
L_DOWN
D32
R257
49.9K
1%
LK_DN
D29
1N914
C299
+15V .1/25
R252
2.2M
R254
2.2M
U55
D28
BAR35
R253
18.2K
1%
74ACT04
LF353
U56
-15V
C301
47/16
R263
4.99K
1%
R262
4.99K
1%

SPARES

U55
74ACT04
U57
74HCU04
NC

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE: SCHEM,MAIN BD,MC4/MC8
PHASE LOCK LOOP

SIZE	CODE	NUMBER	REV
B		060-15259	5

FILE NAME: 15259-6.10 SHEET 10 OF 23

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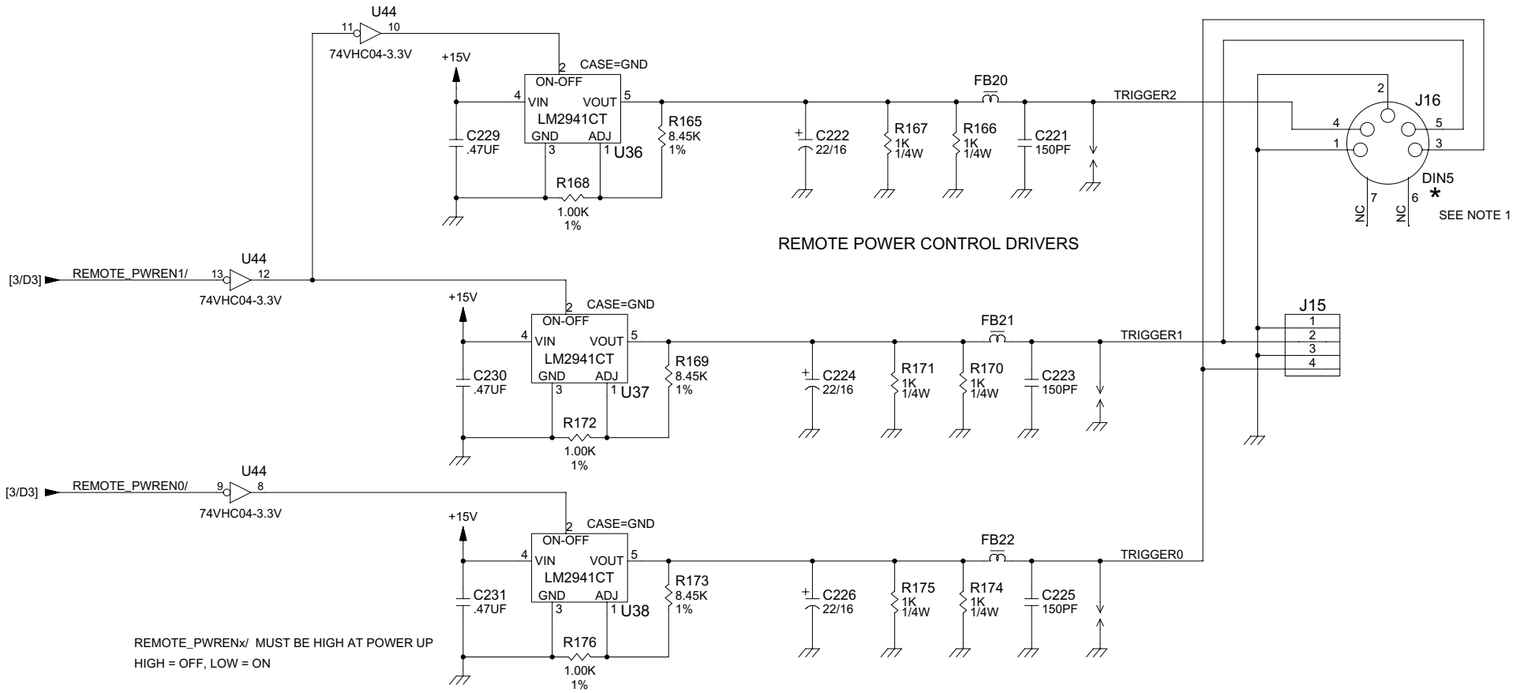
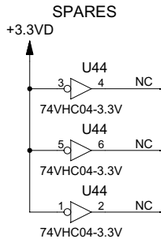
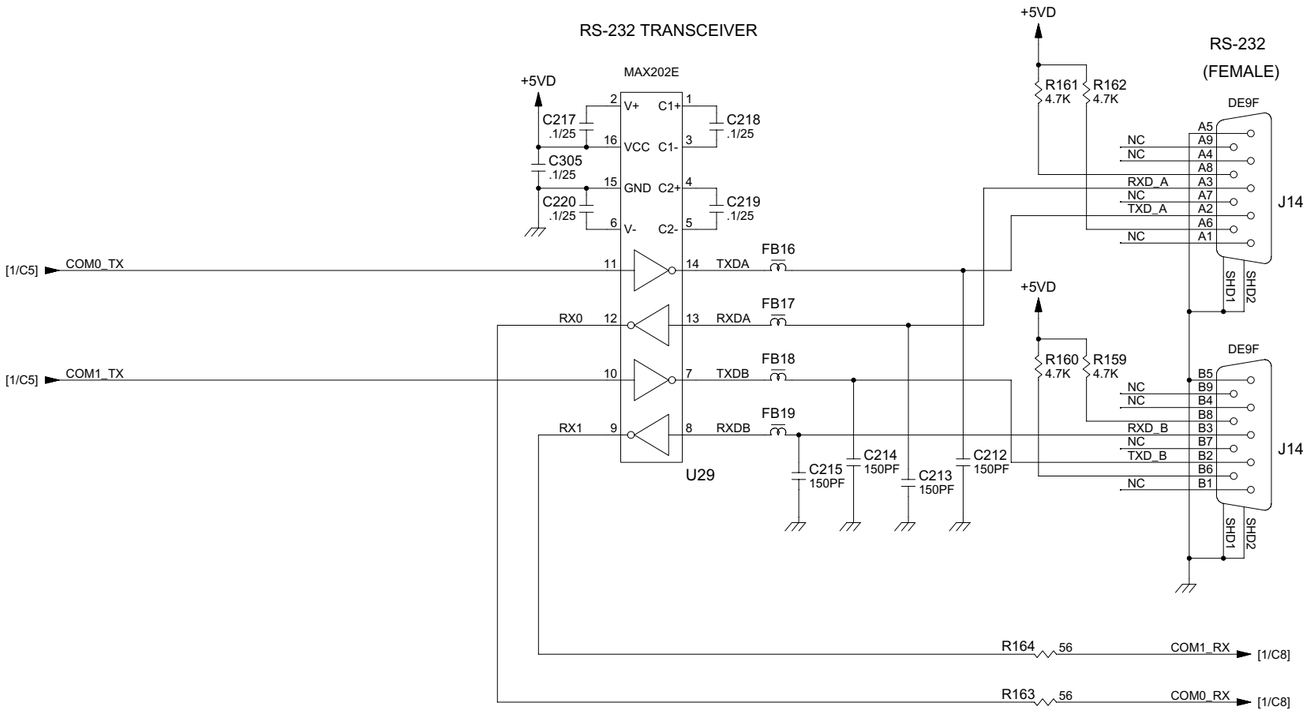




REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



NOTES

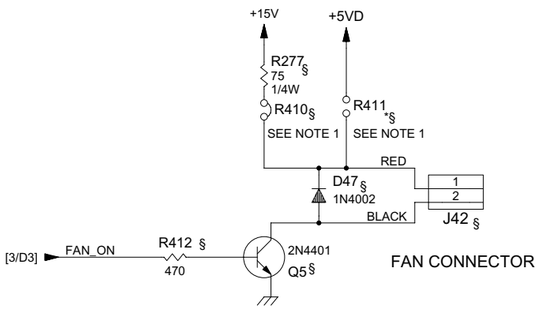
1. INSTALL FOR JBL PRODUCTS ONLY.

RS-232 PINOUT (MALE)

1...DCD	6...DSR
2...RXD	7...RTS
3...TXD	8...CTS
4...DTR	9...RI
5...GND	

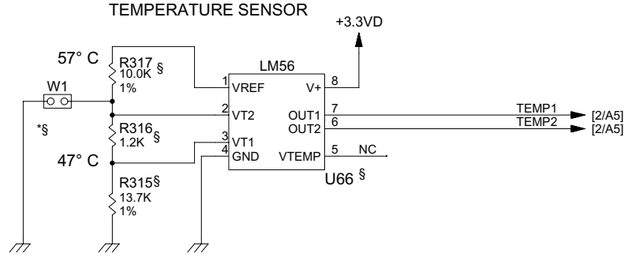
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE SCHEM,MAIN BD,MC4/MC8 REMOTE POWER & RS232 PORTS
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B / CODE / NUMBER 060-15259 / REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.11 / SHEET 11 OF 23

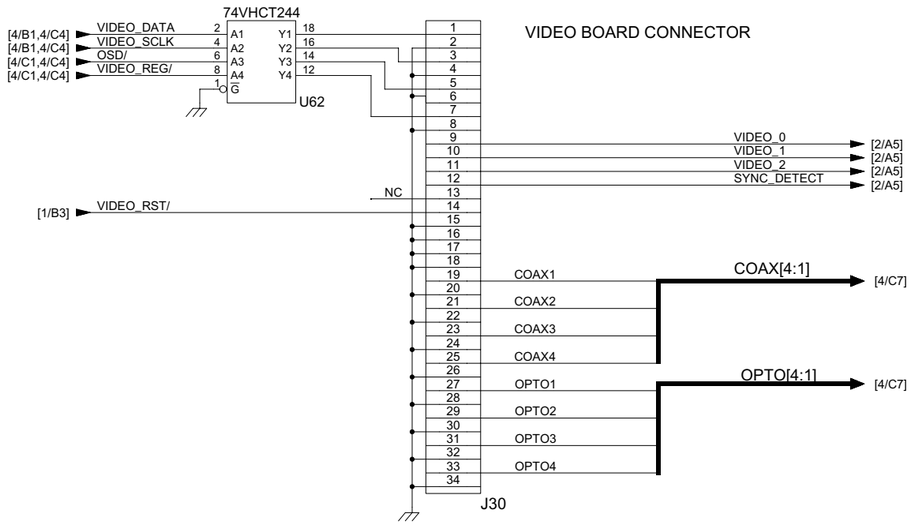
10-19-2004_8:58

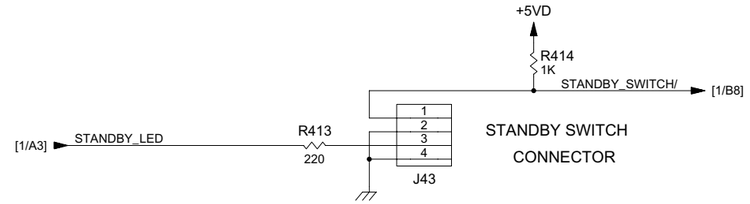


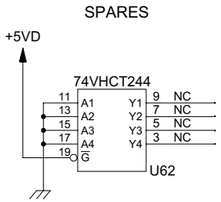
FAN CONNECTOR

TEMPERATURE SENSOR





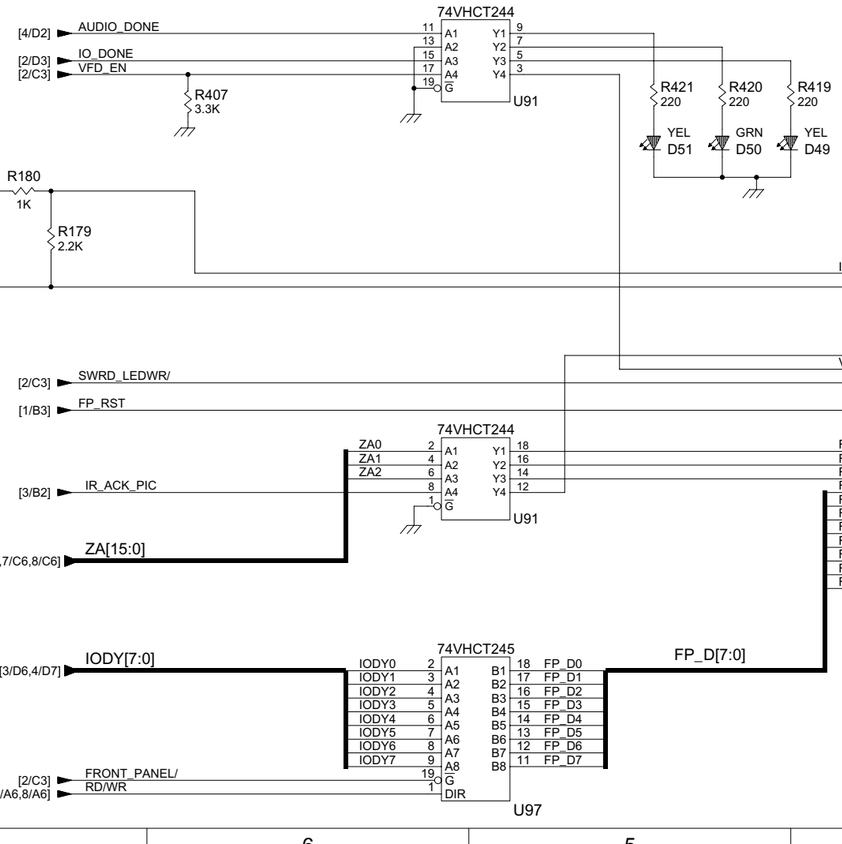




REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

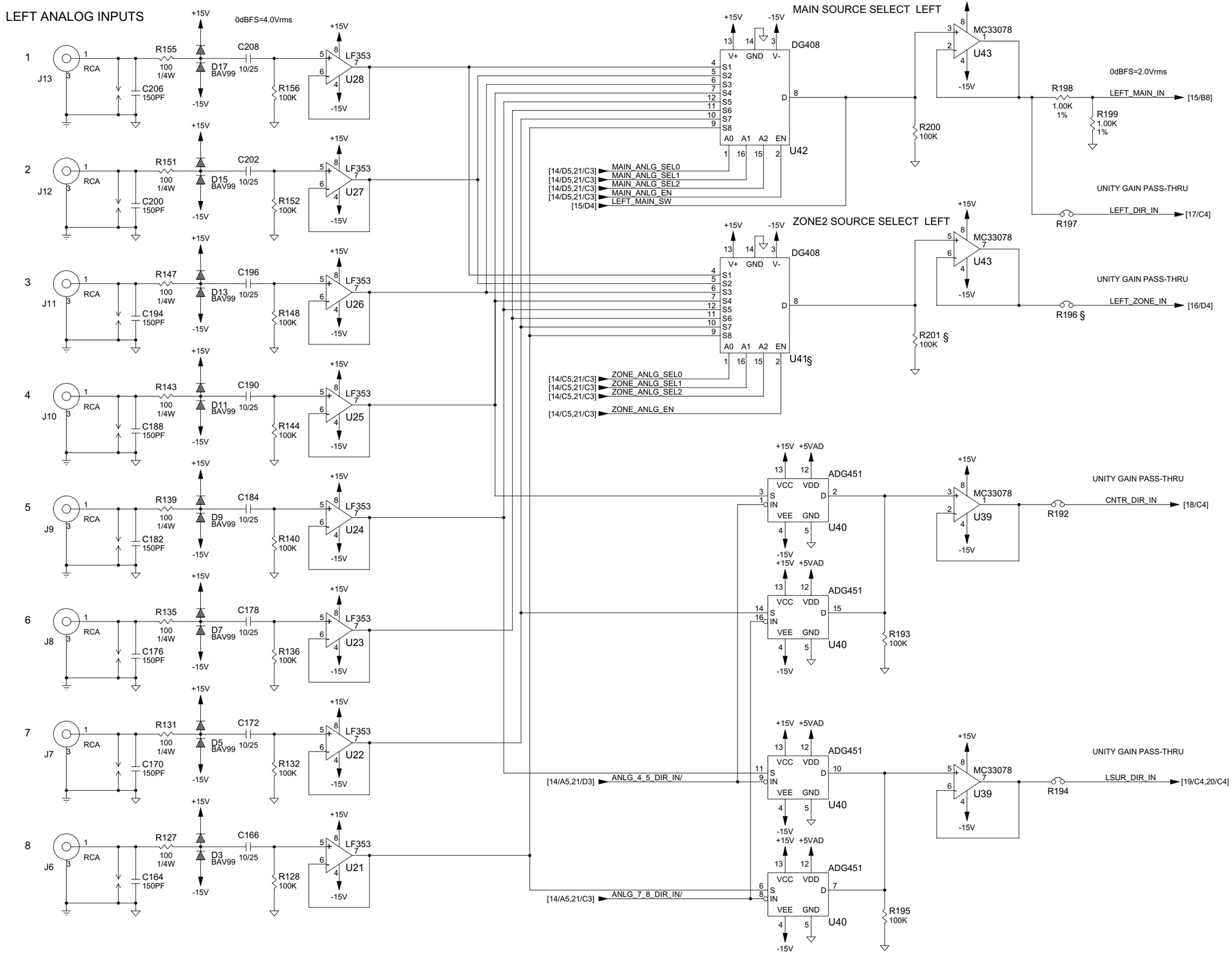
NOTES

1 INSTALL R410 FOR 12V FAN. INSTALL R411 FOR 5V FAN.



CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE SCHEM,MAIN BD,MC4/MC8 FRONT PANEL,STANDBY,VIDEO CONN	
DRAWN RWH	2/15/02	SIZE B / CODE / NUMBER 060-15259 / REV 4	
CHECKED CV	3/29/02		
Q.C. CW	4/3/02		
ISSUED KAB	4/3/02	FILE NAME 15259-6.12	SHEET 12 OF 23

10-19-2004 9:02



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	CHANGED U21-28 PER ECO 030213-00	RWH 02/19/03	CW 02/20/03
		CBV 02/19/03	KB 02/20/03
5	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

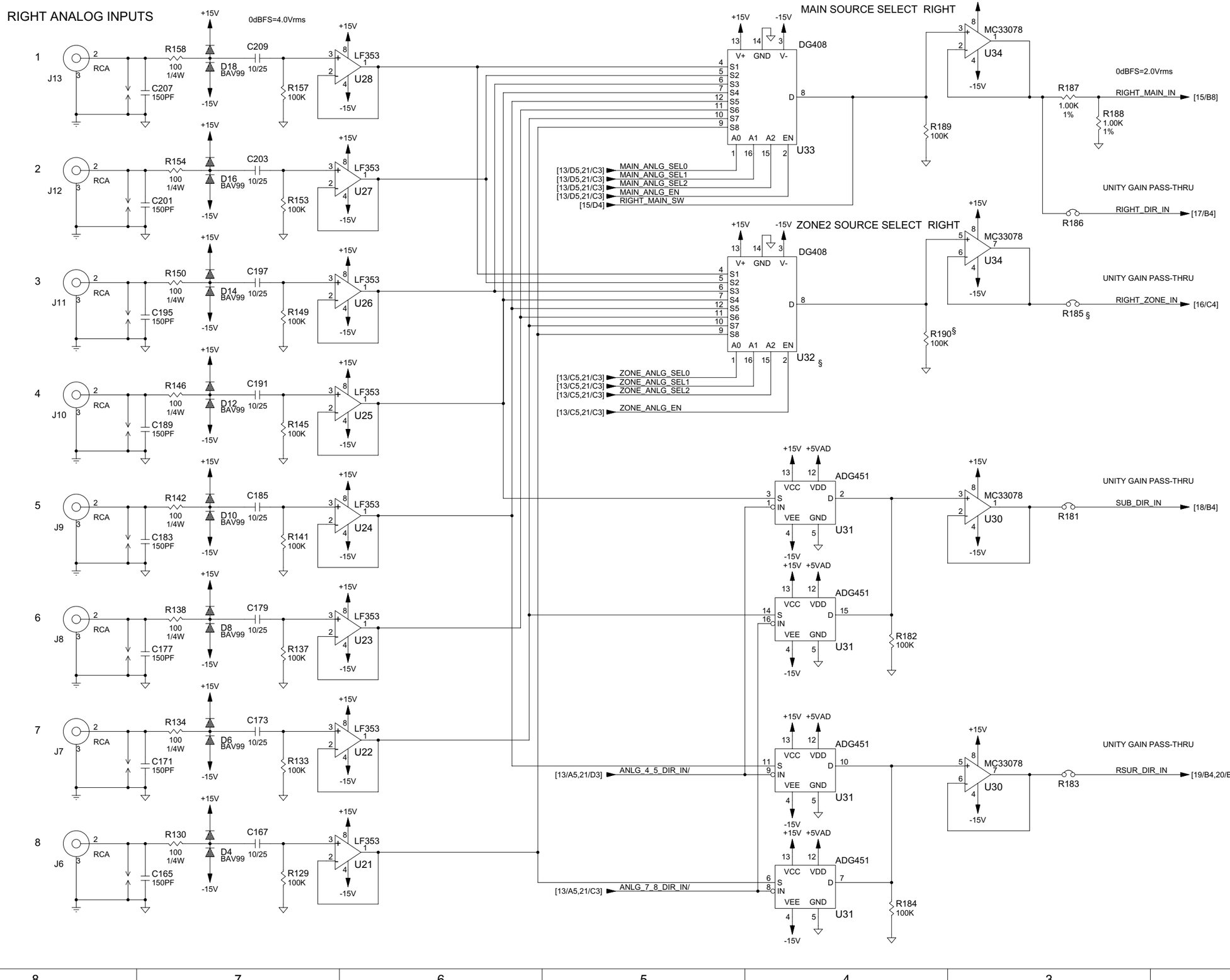
APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE
SCHEM,MAIN BD,MC4/MC8
LEFT ANALOG INPUT MUXES

SIZE	CODE	NUMBER	REV
B		060-15259	5

FILE NAME 15259-6.13
SHEET 13 OF 23

10-19-2004_8:58



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	CHANGED U21-28 PER ECO 030213-00	RWH 02/19/03	CW 02/20/03
		CBV 02/19/03	KB 02/20/03
5	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

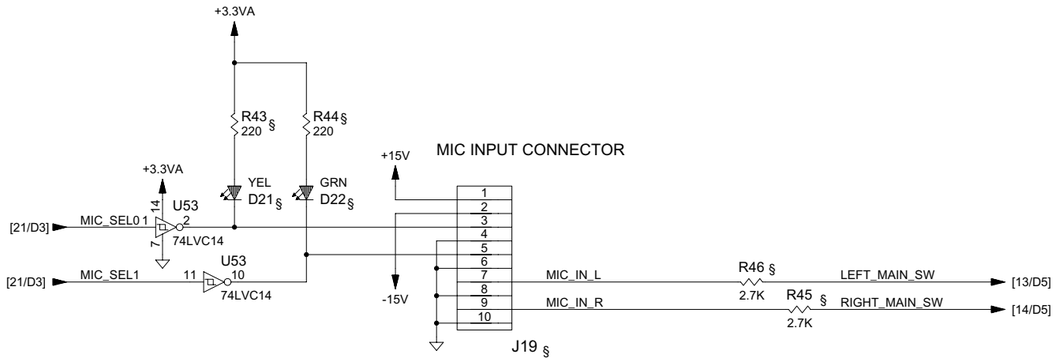
TITLE
SCHEM,MAIN BD,MC4/MC8
RIGHT ANALOG INPUT MUXES

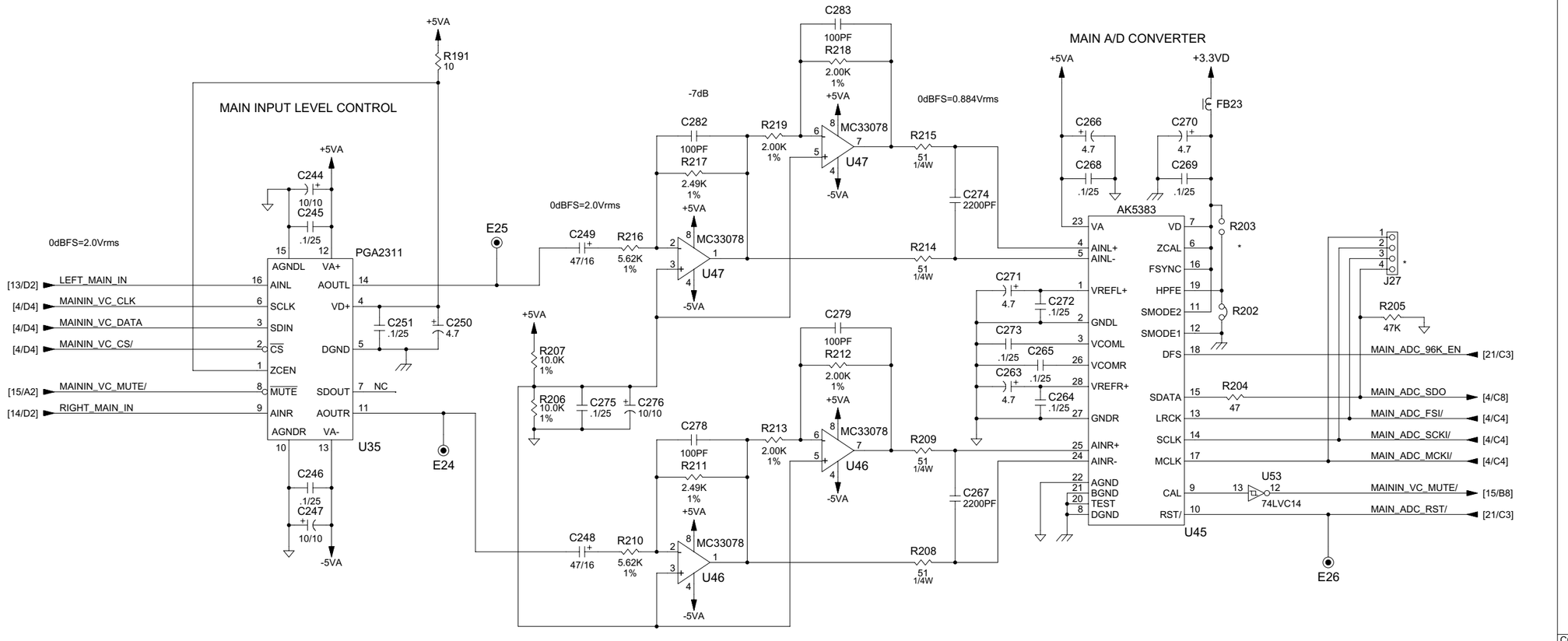
SIZE	CODE	NUMBER	REV
B		060-15259	5

FILE NAME 15259-6.14 SHEET 14 OF 23

10-19-2004 9:04

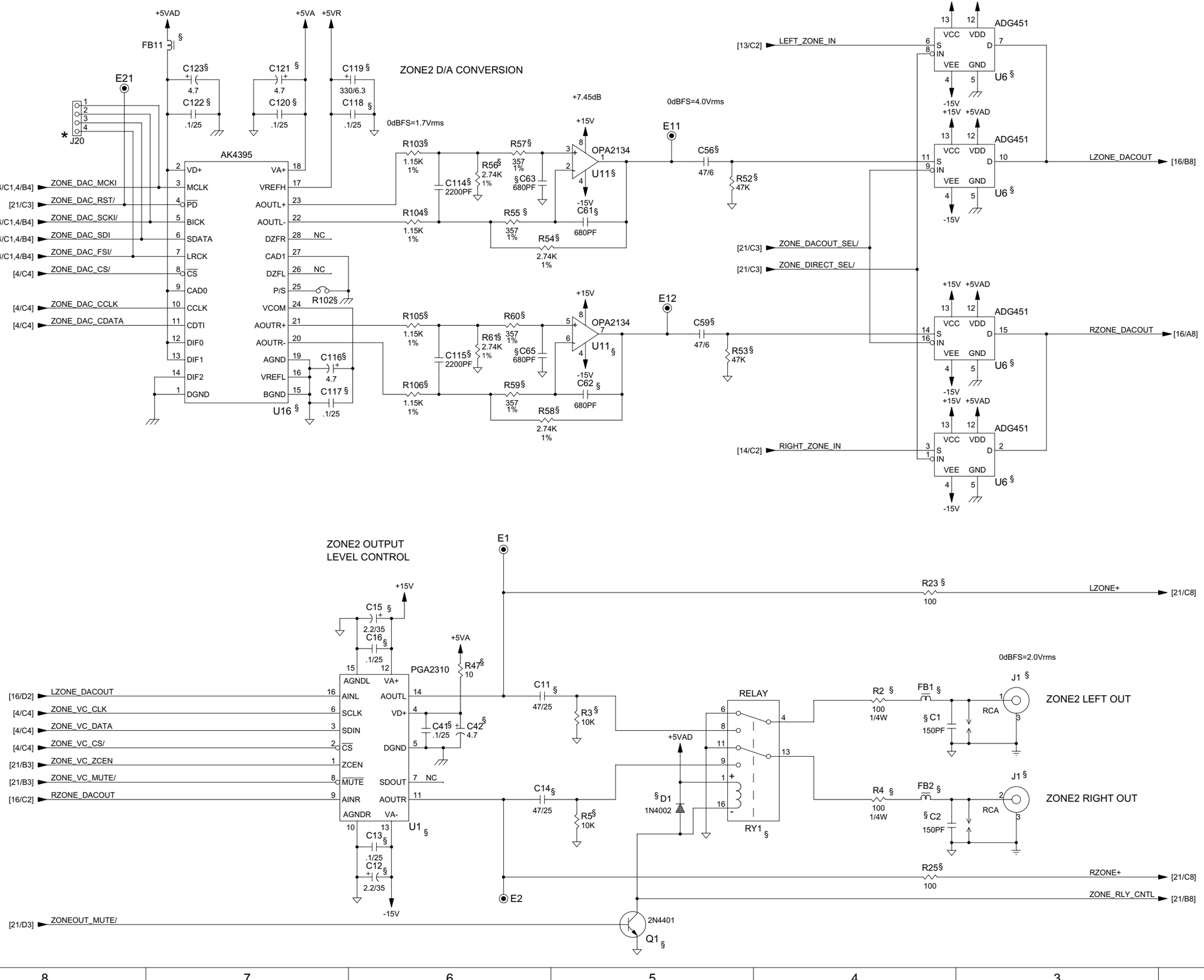
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04





CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 MIC INPUTS & MAIN A/D CONVERTER
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B / CODE / NUMBER 060-15259 / REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.15 / SHEET 15 OF 23

10-19-2004_9:04



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 COMPONENTS ON THIS PAGE ARE NOT INSTALLED ON MC4

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 ZONE2 DAC
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE: B; CODE: ; NUMBER: 060-15259; REV: 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME: 15259-6.16; SHEET: 16 OF 23

10-21-2004 8:20

LEFT & RIGHT FRONT D/A CONVERSION

+5VAD FB15 C163 4.7 C162 .1/25 +5VA +5VR C161 4.7 C160 .1/25 C159 330/6.3 C158 .1/25

J24 1 2 3 4

AK4395 U20

VD+ 2 · MCLK 3 · PD 4 · BICK 5 · SDATA 6 · LRCK 7 · CS 8 · CAD0 9 · CCLK 10 · CDTI 11 · DIF0 12 · DIF1 13 · DIF2 14 · DGND 1

VA+ 18 · VREFH 17 · AOUTL+ 23 · AOUTL- 22 · DZFR 28 NC · CAD1 27 · DZFL 26 NC · P/S 25 R123 · VCOM 24 · AOUTR+ 21 · AOUTR- 20 · AGND 19 · VREFL 16 · BGND 15

C156 4.7 · C157 .1/25

[4/C2] FRONT_DAC_MCKI
[21/B4] FRONT_DAC_RST/
[4/C1,4/C2,18/D8] MAIN_DAC_SCKI0/
[4/C1,4/C4] FRONT_DAC_SDI
[4/C1,4/C2,18/C8] MAIN_DAC_FSI0/
[4/C4] FRONT_DAC_CS/
[4/C4,18/C8,19/C8,20/C8] MAIN_DAC_CCLK
[4/C4,18/C8,19/C8,20/C8] MAIN_DAC_CDATA

0dBFS=1.7Vrms

R122 1.21K 1% · C110 330/6.3 · R96 5.76K 1% · C154 1500PF · R97 280 1% · C95 220PF

R124 1.21K 1% · C111 330/6.3 · R95 280 1% · R94 49.9K 1% · C93 220PF · R92 6.49K 1%

R125 1.21K 1% · C112 330/6.3 · R101 5.76K 1% · C155 1500PF · R100 280 1% · C97 220PF

R126 1.21K 1% · C113 330/6.3 · R99 280 1% · R98 49.9K 1% · C94 220PF · R93 6.49K 1%

+13.5dB

+15V OPA2134 U15 -15V

0dBFS=8Vrms

E19 E20

+15V +5VAD ADG451 U10 -15V

[13/D2] LEFT_DIR_IN
[21/A3] FRONT_DACOUT_SEL/
[21/A3] FRONT_DIRECT_SEL/
[14/D2] RIGHT_DIR_IN

LFRONT_DACOUT [17/B8]
RFRONT_DACOUT [17/A8]

[18/A3,19/B8,20/B8] MAIN_RLY_CNTL

LEFT & RIGHT FRONT LEVEL CONTROL

E9 E10

+15V C39 2.2/35 C40 .1/25 +5VA R51 10

PGA2310 U5

AGNDL 15 · VA+ 12 · AINL 16 · AOUTL 14 · SCLK 6 · VD+ 4 · SDIN 3 · CS 2 · DGND 5 · ZCEN 1 · MUTE 8 · SDOUT 7 NC · AINR 9 · AOUTR 11 · AGNDR 10 · VA- 13

C53 .1/25 · C54 4.7 · C37 .1/25 · C36 2.2/35 · -15V

[17/D3] LFRONT_DACOUT
[4/D4,18/B8,19/B8,20/B8] MAINOUT_VC_CLK
[4/C4,18/B8,19/B8,20/A8] MAINOUT_VC_DATA
[4/D4] FRONT_VC_CS/
[21/B3] FRONT_VC_ZCEN
[21/A3] FRONT_VC_MUTE/
[17/C3] RFRONT_DACOUT

C35 47/25 · R19 10K · C38 47/25 · R21 10K

RELAY RY5 +5VAD

R39 100 LFRONT+ [21/C8]

R41 100 RFRONT+ [21/C8]

0dBFS=8.1Vrms

R18 100 1/4W · FB9 · C9 150PF · J5 LEFT FRONT OUT RCA

R20 100 1/4W · FB10 · C10 150PF · J5 RIGHT FRONT OUT RCA

REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

Lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

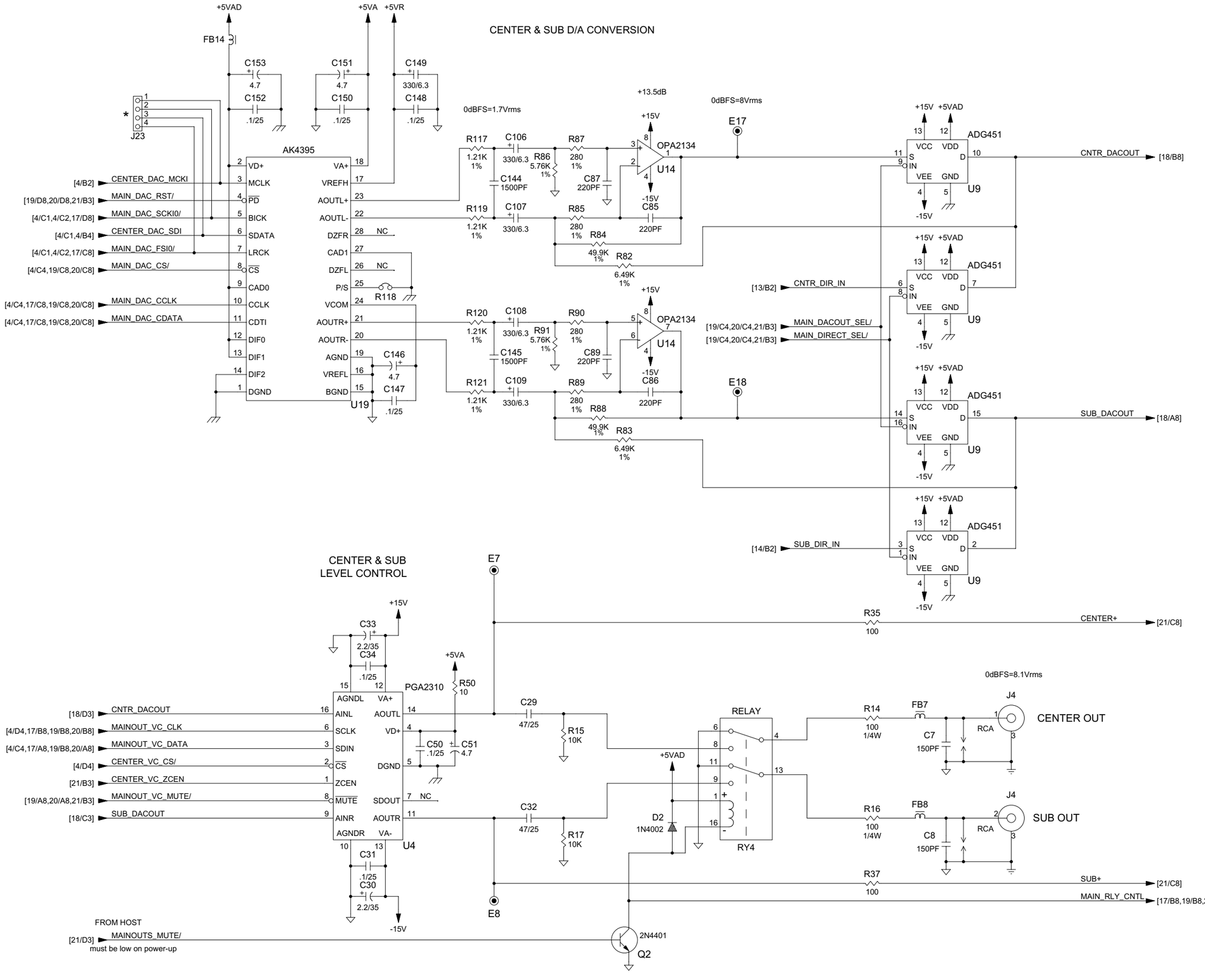
TITLE: SCHEM,MAIN BD,MC4/MC8 L/R FRONT DACS

SIZE B | CODE | NUMBER 060-15259 | REV 4

FILE NAME 15259-6.17 SHEET 17 OF 23

10-19-2004_8:58

CENTER & SUB D/A CONVERSION



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE: SCHEM,MAIN BD,MC4/MC8 CENTER/SUB DACS

SIZE	CODE	NUMBER	REV
B		060-15259	4

FILE NAME: 15259-6.18 SHEET 18 OF 23

10-19-2004_8:58

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

LEFT & RIGHT SIDE D/A CONVERSION

+5VAD, +5VA, +5VR
FB13
C143 4.7, C142 .1/25
C141 4.7, C140 .1/25
C139 330/6.3, C138 .1/25
J22
AK4395
[4/B2] SIDE_DAC_MCKI
[18/D8,20/D8,21/B3] MAIN_DAC_RST/
[4/C1,4/C2,20/D8] MAIN_DAC_SCKI1/
[4/C1,4/B4] SIDE_DAC_SDI
[4/C1,4/C2,20/C8] MAIN_DAC_FSI1/
[4/C4,18/C8,20/C8] MAIN_DAC_CS/
[4/C4,17/C8,18/C8,20/C8] MAIN_DAC_CCLK
[4/C4,17/C8,18/C8,20/C8] MAIN_DAC_CDATA
VD+, MCLK, PD, BICK, SDATA, LRCK, CS, CAD0, CCLK, CDTI, DIF0, DIF1, DIF2, DGND
VA+, VREFH, AOUTL+, AOUTL-, DZFR, CAD1, DZFL, P/S, VCOM, AOUTR+, AOUTR-, AGND, VREFL, BGND
C136 4.7, C137 .1/25
U18
+13.5dB
0dBFS=1.7Vrms
R112 1.21K 1%, C102 330/6.3, R76 5.76K 1%, R77 280 1%, C134 1500PF, C79 220PF
R114 1.21K 1%, C103 330/6.3, R75 280 1%, R74 49.9K 1%, C77 220PF, R72 6.49K 1%
R115 1.21K 1%, C104 330/6.3, R81 5.76K 1%, R80 280 1%, C135 1500PF, C81 220PF
R116 1.21K 1%, C105 330/6.3, R79 280 1%, R78 49.9K 1%, C78 220PF, R73 6.49K 1%
+15V, -15V, OPA2134, U13
0dBFS=8Vrms
E15, E16
[13/A2,20/C4] LSUR_DIR_IN
[18/C4,20/C4,21/B3] MAIN_DACOUT_SEL/
[18/C4,20/C4,21/B3] MAIN_DIRECT_SEL/
[14/A2,20/B4] RSUR_DIR_IN
ADG451, VCC, VDD, S, IN, D, VEE, GND, U8
LSIDE_DACOUT [19/B8]
RSIDE_DACOUT [19/A8]
[17/B8,18/A3,20/B8] MAIN_RLY_CNTL

LEFT & RIGHT SIDE LEVEL CONTROL

E5, E6
R31 100, LSIDE+ [21/C8]
R33 100, RSIDE+ [21/C8]
+15V, -15V, +5VA, +5VAD
C27 2.2/35, C28 .1/25, C25 .1/25, C24 2.2/35
PGA2310, U3
[19/D3] LSIDE_DACOUT
[4/D4,17/B8,18/B8,20/B8] MAINOUT_VC_CLK
[4/C4,17/A8,18/B8,20/A8] MAINOUT_VC_DATA
[4/D4] SIDE_VC_CS/
[21/B3] SIDE_VC_ZCEN
[18/A8,20/A8,21/B3] MAINOUT_VC_MUTE/
[19/C3] RSIDE_DACOUT
AGNDL, VA+, AINL, AOUTL, SCLK, VD+, SDIN, CS, DGND, ZCEN, MUTE, SDOUT, AINR, AOUTR, AGNDR, VA-
R49 10, C47 .1/25, C48 4.7
C23 47/25, R11 10K, C26 47/25, R13 10K
RELAY, RY3
0dBFS=8.1Vrms
R10 100 1/4W, FB5, C5 150PF, J3, RCA, LEFT SIDE OUT
R12 100 1/4W, FB6, C6 150PF, J3, RCA, RIGHT SIDE OUT

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 L/R SIDE DACS
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B; CODE; NUMBER 060-15259; REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.19; SHEET 19 OF 23

10-19-2004_8:58

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

LEFT & RIGHT REAR D/A CONVERSION

+5VAD, +5VA, +5VR
FB12
C133 4.7, C132 .1/25
C131 4.7, C130 .1/25
C129 330/6.3, C128 .1/25
J21
AK4395
[4/B2] REAR_DAC_MCKI
[18/D8,19/D8,21/B3] MAIN_DAC_RST/
[4/C1,4/C2,19/D8] MAIN_DAC_SCKI1/
[4/C1,4/B4] REAR_DAC_SDI
[4/C1,4/C2,19/C8] MAIN_DAC_FSI1/
[4/C4,18/C8,19/C8] MAIN_DAC_CS/
[4/C4,17/C8,18/C8,19/C8] MAIN_DAC_CCLK
[4/C4,17/C8,18/C8,19/C8] MAIN_DAC_CDATA
VD+, MCLK, PD, BICK, SDATA, LRCK, CS, CAD0, CCLK, CDTI, DIF0, DIF1, DIF2, DGND
VA+, VREFH, AOUTL+, AOUTL-, DZFR, CAD1, DZFL, P/S, VCOM, AOUTR+, AOUTR-, AGND, VREFL, BGND
NC, NC
R108
C126 4.7, C127 .1/25
U17

+13.5dB
0dBFS=1.7Vrms
R107 1.21K 1%, C98 330/6.3, R66 5.76K 1%, R67 280 1%, C124 1500PF, C71 220PF
R109 1.21K 1%, C99 330/6.3, R65 280 1%, R64 49.9K 1%, R62 6.49K 1%, C69 220PF
+15V, -15V, OPA2134, U12
0dBFS=8Vrms
E13

R110 1.21K 1%, C100 330/6.3, R70 280 1%, R71 5.76K 1%, C125 1500PF, C73 220PF
R111 1.21K 1%, C101 330/6.3, R69 280 1%, R68 49.9K 1%, R63 6.49K 1%, C70 220PF
OPA2134, U12
E14

ADG451, U7
+15V, +5VAD, -15V
[13/A2,19/C4] LSUR_DIR_IN
[18/C4,19/C4,21/B3] MAIN_DACOUT_SEL/
[18/C4,19/C4,21/B3] MAIN_DIRECT_SEL/
[14/A2,19/B4] RSUR_DIR_IN
LREAR_DACOUT [20/B8]
RREAR_DACOUT [20/A8]

[17/B8,18/A3,19/B8] MAIN_RLY_CNTL

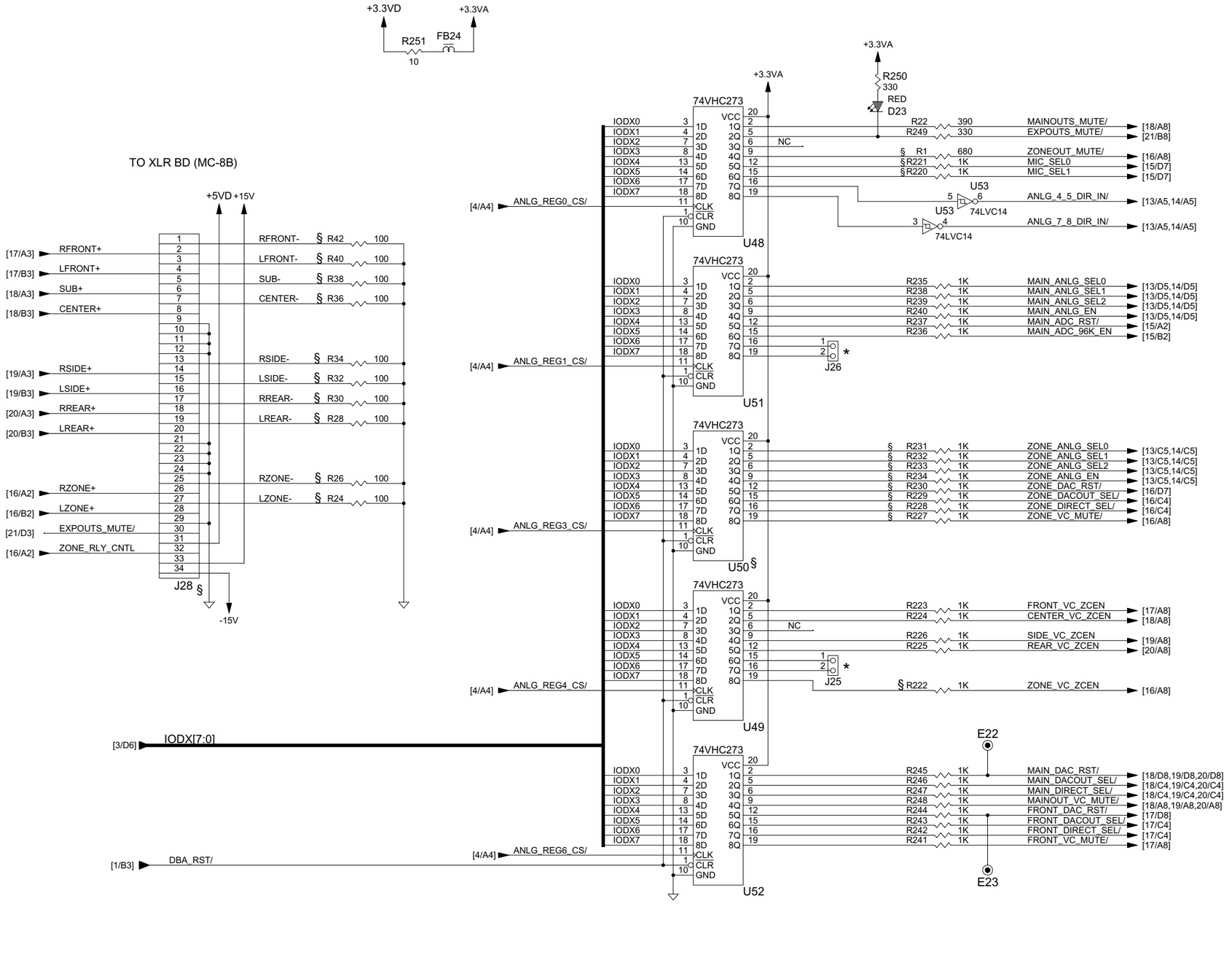
LEFT & RIGHT REAR LEVEL CONTROL

E3, E4
+15V, -15V
C21 2.2/35, C22 .1/25
C19 .1/25, C18 2.2/35
+5VA
R48 10
PGA2310, U2
[20/D3] LREAR_DACOUT
[4/D4,17/B8,18/B8,19/B8] MAINOUT_VC_CLK
[4/C4,17/A8,18/B8,19/B8] MAINOUT_VC_DATA
[4/D4] REAR_VC_CS/
[21/B3] REAR_VC_ZCEN
[18/A8,19/A8,21/B3] MAINOUT_VC_MUTE/
[20/C3] RREAR_DACOUT
AGNDL, AINL, SCLK, SDIN, CS, ZCEN, MUTE, AINR, AGNDR
VA+, AOUTL, VD+, DGND, SDOUT, AOUTR, VA-
NC
C44 .1/25, C45 4.7
C17 47/25, C20 47/25
R7 10K, R9 10K
+5VAD
RELAY, RY2
R27 100, R29 100
LREAR+ [21/C8]
RREAR+ [21/C8]
0dBFS=8.1Vrms
R6 100 1/4W, R8 100 1/4W
FB3, FB4
C3 150PF, C4 150PF
J2, RCA
LEFT REAR OUT
RIGHT REAR OUT

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 L/R REAR DACS
DRAWN	RWH	2/15/02	
CHECKED	CV	3/29/02	SIZE B; CODE; NUMBER 060-15259; REV 4
Q.C.	CW	4/3/02	
ISSUED	KAB	4/3/02	FILE NAME 15259-6.20; SHEET 20 OF 23

10-19-2004 8:58

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,MAIN BD,MC4/MC8 XLR BD CONN,CONTROL REG
DRAWN RWH	2/15/02	SIZE B | CODE | NUMBER 060-15259 | REV 4
CHECKED CV	3/29/02	
Q.C. CW	4/3/02	FILE NAME 15259-6.21 | SHEET 21 OF 23
ISSUED KAB	4/3/02	

10-19-2004_8:58

AC INPUT

REAR PANEL POWER SWITCH

NEUTRAL

LINE

FERRITE SLEEVE 1.5 TURNS

NC

POWER SUPPLY 80W

+5V @ 10A
-5V @ 0.8A
+15V @ 3.0A
-15V @ 0.8A

FERRITE SLEEVE 1.5 TURNS

TO MAIN BD, DIGITAL J31

TO MAIN BD, ANALOG J26

ANALOG POWER

+5VAD SOURCE

FB29 2.5TURN

C321 .22/50 C320 150PF 100/25 C310 C309 .22/50 C308 150PF

D34 1A

1K R278

IRL3803 Q3

-5VA SOURCE

C323 .22/50 C322 150PF FB30 2.5TURN 100/25 C311 C312 .22/50 C313 150PF

D36 1N4002

FROM POWER SUPPLY

J32

+15V SOURCE

FB31 2.5TURN

C325 .22/50 C324 150PF 100/25 C316 C314 .22/50 C315 150PF

GNDA

-15V SOURCE

D35 1A C327 .22/50 C326 150PF FB32 2.5TURN 100/25 C317 C318 .22/50 C319 150PF

+5VA REGULATOR

1N4002 D38

7805 U63

C330 .1/25 C329 10/10 C328 .1/25

D37 1N4002

-5VA REGULATOR

C331 .1/25 U59 7905

D39 1N4002

C333 .1/25 C332 10/10

D40 1N4002

SEE NOTE 1

TEST POINTS

-15V2 +15V2 +15V3 +5VA3 +3.3VD2

GNDA2 GNDA3 GNDA4 GNDA5 GNDA6 GNDA7 GNDA8 GNDA9 GNDA10 GNDA11

GNDD2 GNDD3 GNDD4 GNDD5 GNDD6 GNDD7 GNDD8 GNDD9 GNDD10 GNDD11

DIGITAL POWER

+5V POWER CONNECTOR

J45

FROM POWER SUPPLY

C410 C409 .22/50 C408 150PF

3.3V REGULATOR

D48 1N4002

LMS1585A TO-220 U96

L1 24UH C402 560/35 C404 .1/25 C403 10/10

+3.3V CONNECTOR - USED ONLY IF ALTERNATE SUPPLY USED

J44

FROM POWER SUPPLY

C405 C406 .22/50 C407 150PF

+5VR REGULATOR

1N4002 D24

C291 .1/25 U60 MC7805

D25 1N4002

E34

J29

TO VIDEO BOARD

REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	CHANGED PWR SUPPLY PER ECO 031111-00	RWH 3/2/04	CW 5/25/04
		GAP 5/18/04	KAB 5/26/04
5	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 INSTALL FOR USE WITH POWER SUPPLIES WITHOUT -5V.

CONTRACT NO.

Lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE: SCHEM,MAIN BD,MC4/MC8 POWER SUPPLY

SIZE B | CODE | NUMBER 060-15259 | REV 5

FILE NAME 15259-6.22 SHEET 22 OF 23

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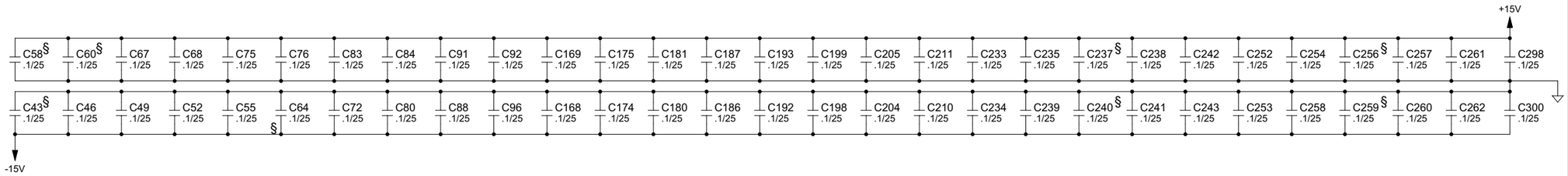
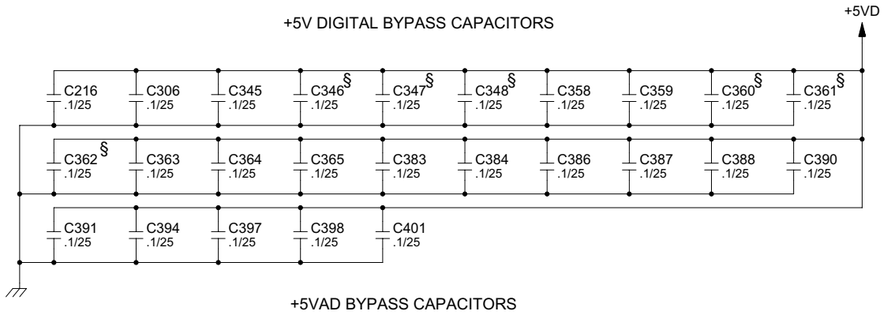
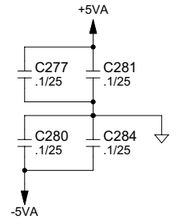
+/-15V BYPASS CAPACITORS



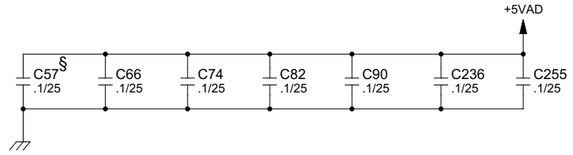
+5V DIGITAL BYPASS CAPACITORS



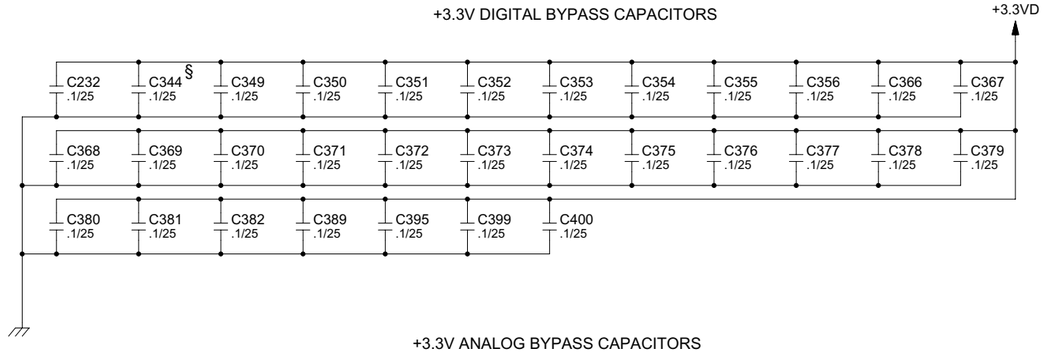
+/-5V ANALOG BYPASS CAPACITORS



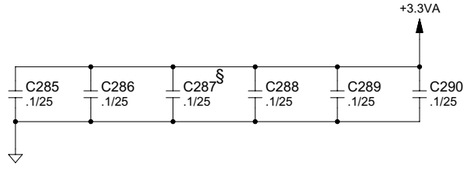
+5VAD BYPASS CAPACITORS



+3.3V DIGITAL BYPASS CAPACITORS



+3.3V ANALOG BYPASS CAPACITORS



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020430-00	RWH 5/16/02	CW 6/24/02
		KB 6/4/02	KB 6/26/02
2	CHANGED PER DCR 020731-00	RWH 8/1/02	CW 8/5/02
		CBV 8/5/02	KB 8/14/02
3	CHANGED PER DCR 020827-00	RWH 8/30/02	CW 9/12/02
		KB 9/12/02	KB 9/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/15/02
CHECKED	CV	3/29/02
Q.C.	CW	4/3/02
ISSUED	KAB	4/3/02

TITLE
SCHEM,MAIN BD,MC4/MC8
BYPASS CAPACITORS

SIZE	CODE	NUMBER	REV
B		060-15259	4

FILE NAME 15259-6.23 SHEET 23 OF 23

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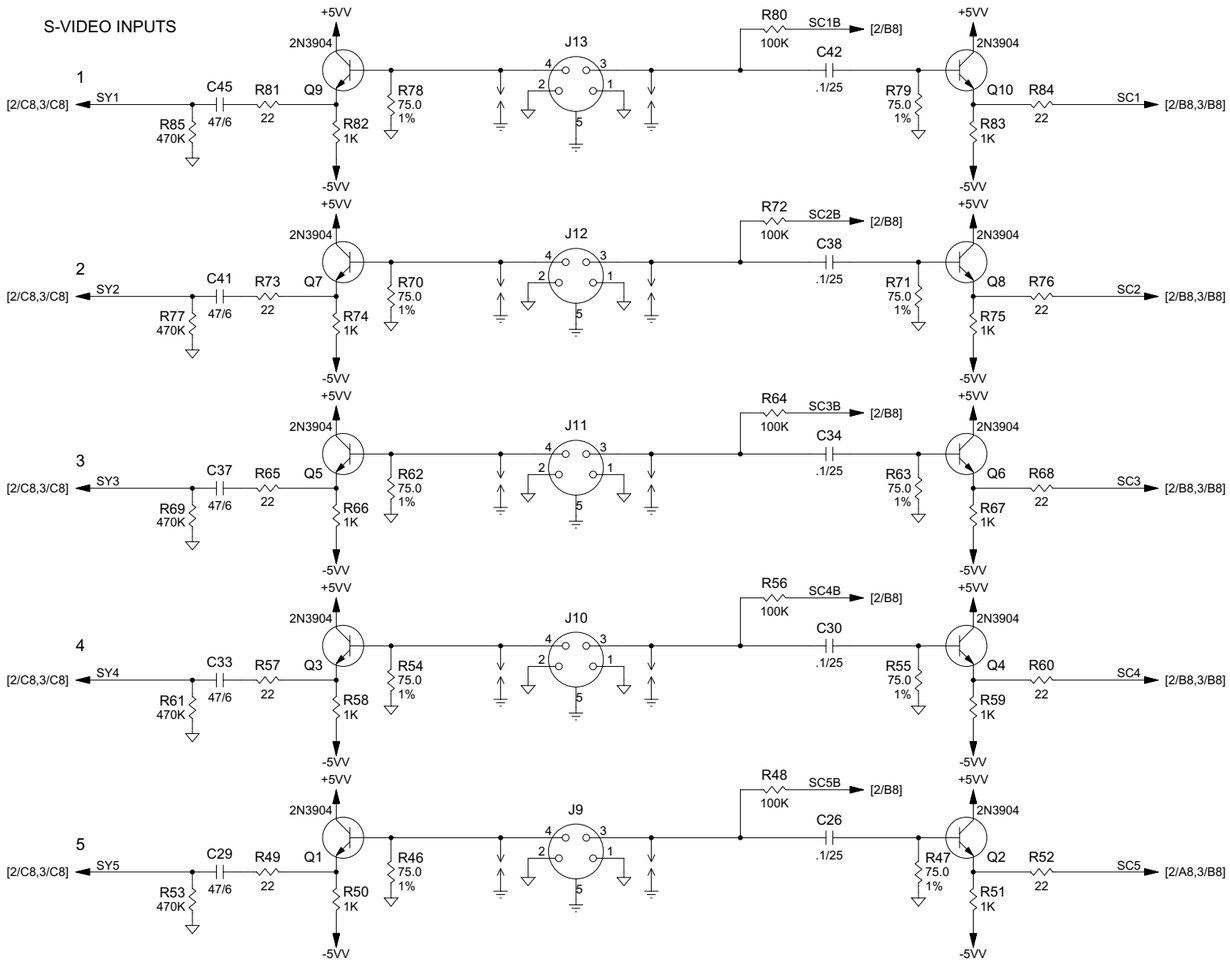


REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	CHANGED SHEETS 3,5 PER DCR 020715-00	CW 8/5/02	RWH 8/14/02
		ECM 8/13/02	KB 8/14/02
3	CHANGED SHEET 4 PER EC0 021105-00	CW 11/11/02	RWH 11/12/02
		ECM 11/12/02	KAB 11/12/02
4	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED ON: C148, CP2, D9, FB4, J19, L1, Q15, R172, RY6, U38, Y1.

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

8 COMPONENTS MARKED WITH § ARE NOT INSTALLED ON MC4.

DOCUMENT CONTROL BLOCK: #060-15269

SHEET	REVISION	TITLE
1 OF 8	4	S-VIDEO INPUTS
2 OF 8	2	MONITOR
3 OF 8	3	ZONE
4 OF 8	3	COMPONENT VIDEO
5 OF 8	3	ON-SCREEN DISPLAY
6 OF 8	2	SYNC STRIPPER
7 OF 8	2	CONTROL REGISTERS
8 OF 8	2	PWR,SPDIF,MAIN&RCA BD CONNS

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

TITLE: SCHEM,VIDEO BD, MC4/MC8
S-VIDEO INPUTS

SIZE	CODE	NUMBER	REV
B		060-15269	4

FILE NAME: 15269-4 .1 SHEET 1 OF 8

OCT 27 2004

RELEASED COPY

10-19-2004_8:43

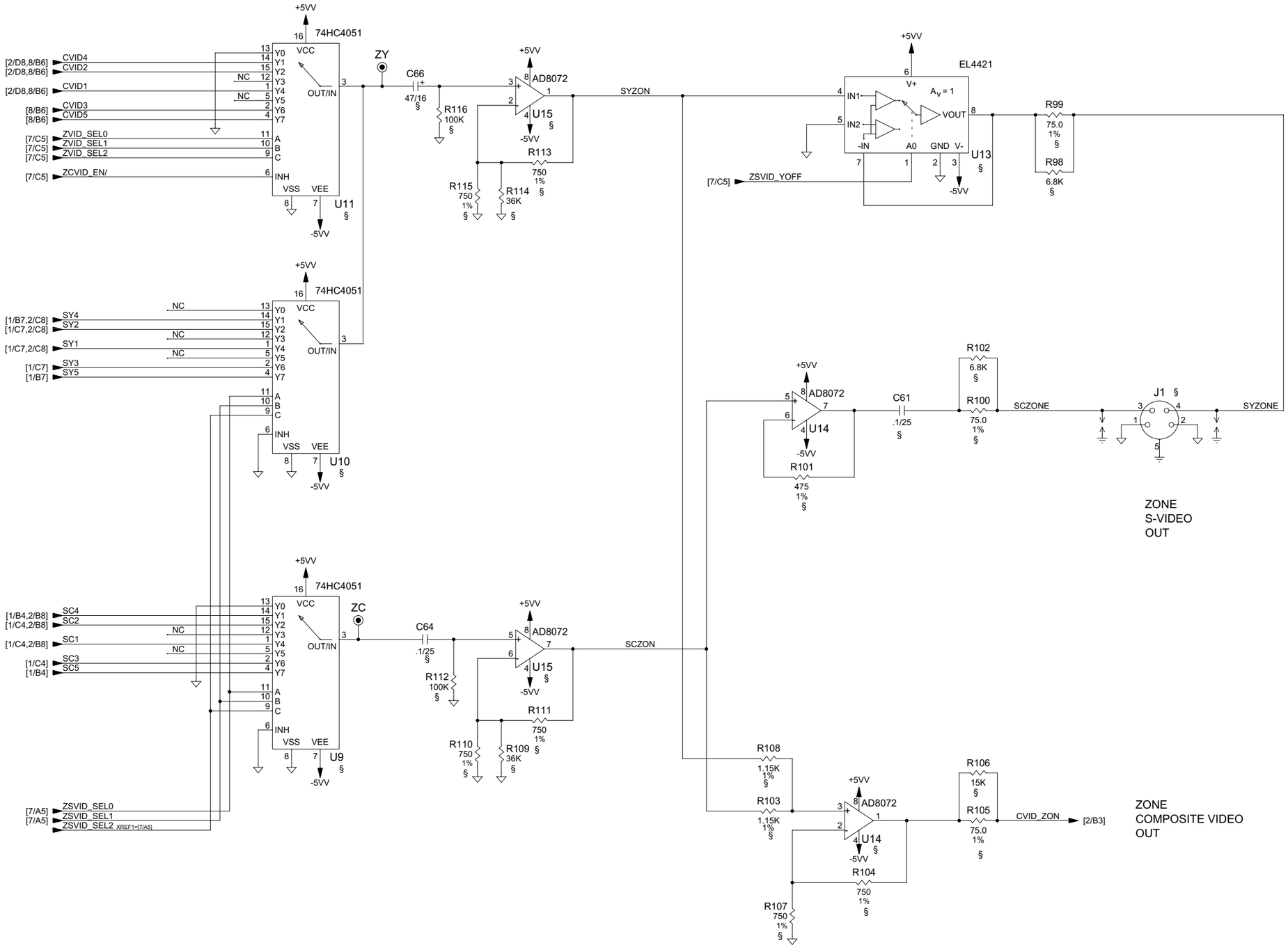
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

MAIN S-VIDEO OUT

COMPOSITE VIDEO OUTPUTS

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, MC4/MC8 MONITOR
DRAWN RWH	3/13/02	SIZE B | CODE | NUMBER 060-15269 | REV 2
CHECKED ECM	3/18/02	
Q.C. CW	3/19/02	
ISSUED KB	3/19/02	FILE NAME 15269-4 .2 | SHEET 2 OF 8

10-19-2004 8:34



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	CHANGED U14,15 PER DCR 020715-00	CW 8/5/02	RWH 8/14/02
		ECM 8/13/02	KB 8/14/02
3	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 COMPONENTS ON THIS PAGE ARE NOT INSTALLED ON MC-4

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

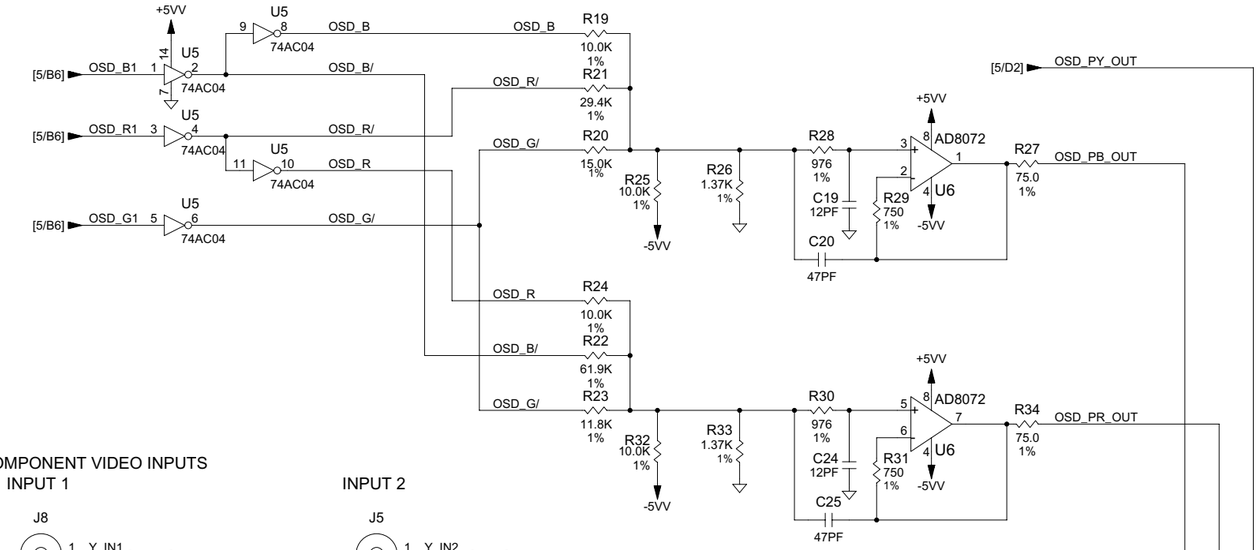
TITLE: SCHEM,VIDEO BD, MC4/MC8
ZONE

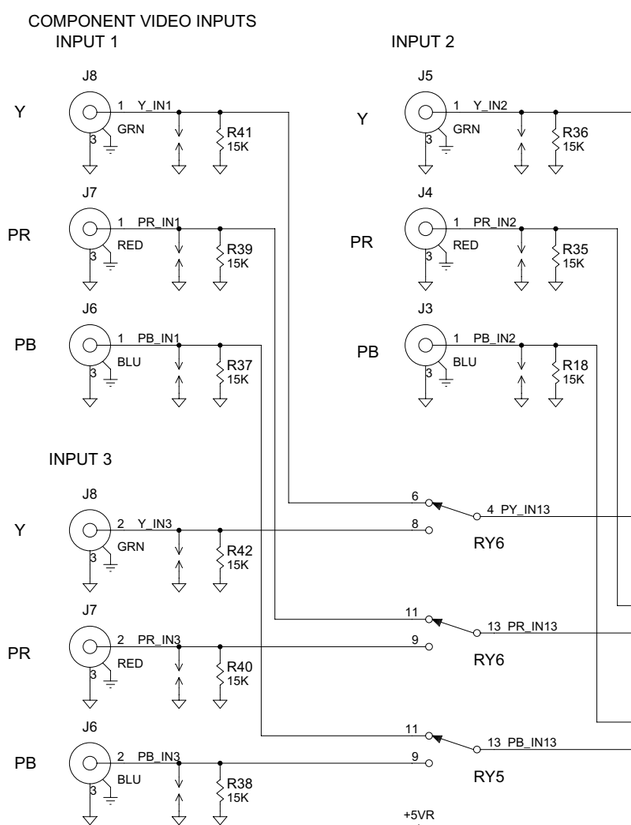
SIZE	CODE	NUMBER	REV
B		060-15269	3

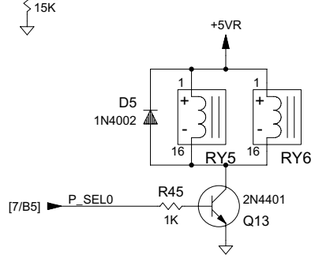
FILE NAME: 15269-4 .3
SHEET 3 OF 8

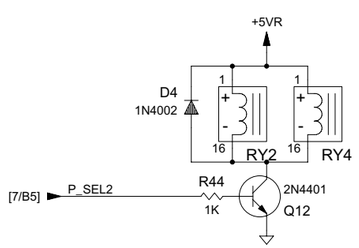
10-21-2004_8:13

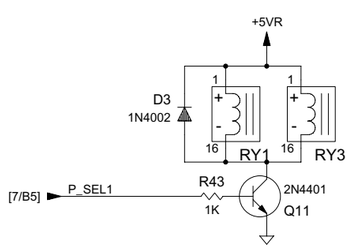
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	USE RY5 SPARE PER ECO 021105-00	CW 11/11/02	RWH 11/12/02
		ECM 11/12/02	KAB 11/12/02
3	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

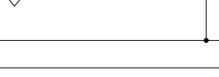




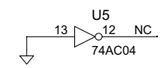


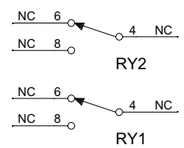






SPARES





CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

TITLE: SCHEM,VIDEO BD, MC4/MC8 COMPONENT VIDEO

SIZE	CODE	NUMBER	REV
B		060-15269	3

FILE NAME: 15269-4 .4 SHEET 4 OF 8

10-19-2004 8:34

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	CHANGED U24 PER DCR 020715-00	CW 8/5/02	RWH 8/14/02
		ECM 8/13/02	KB 8/14/02
3	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

SPARES

+5VV AD8072 U25 -5VV

ON-SCREEN DISPLAY

FILTERS

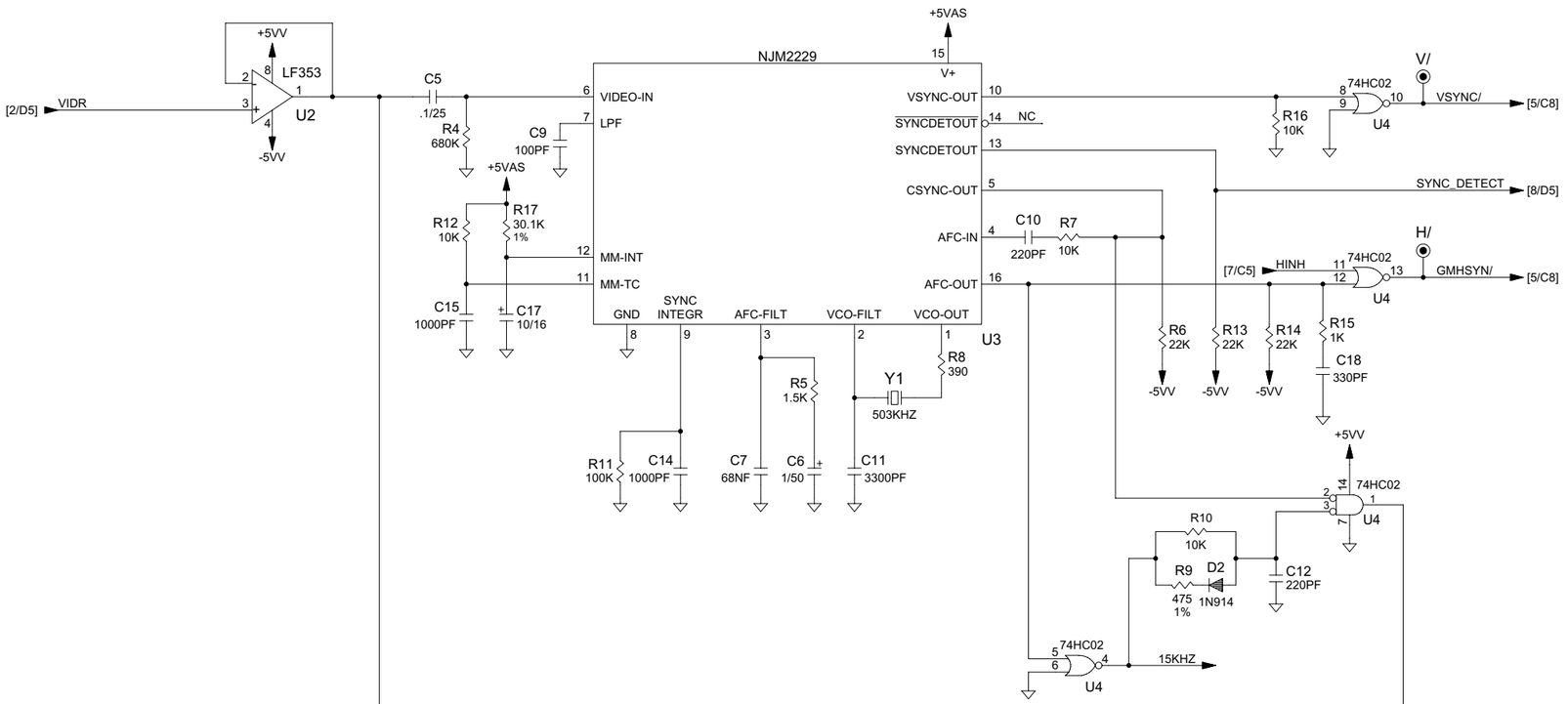
4XFSC OSCILLATORS

FONT MEMORY

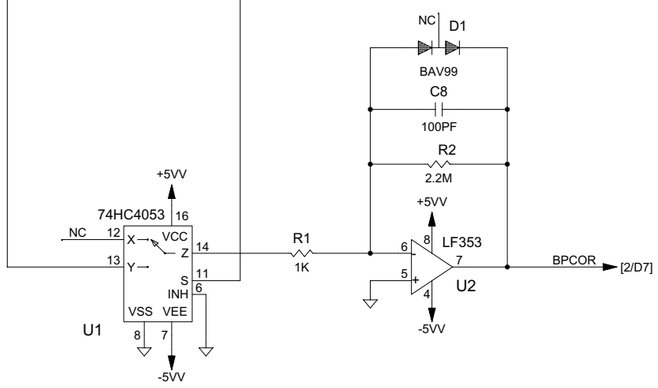
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO BD, MC4/MC8 ON-SCREEN DISPLAY	
DRAWN RWH	3/13/02	SIZE B	CODE
CHECKED ECM	3/18/02	NUMBER 060-15269	REV 3
Q.C. CW	3/19/02	FILE NAME 15269-4.5	SHEET 5 OF 8
ISSUED KB	3/19/02		

10-19-2004_8:34

SYNC STRIPPER



DC RESTORER



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

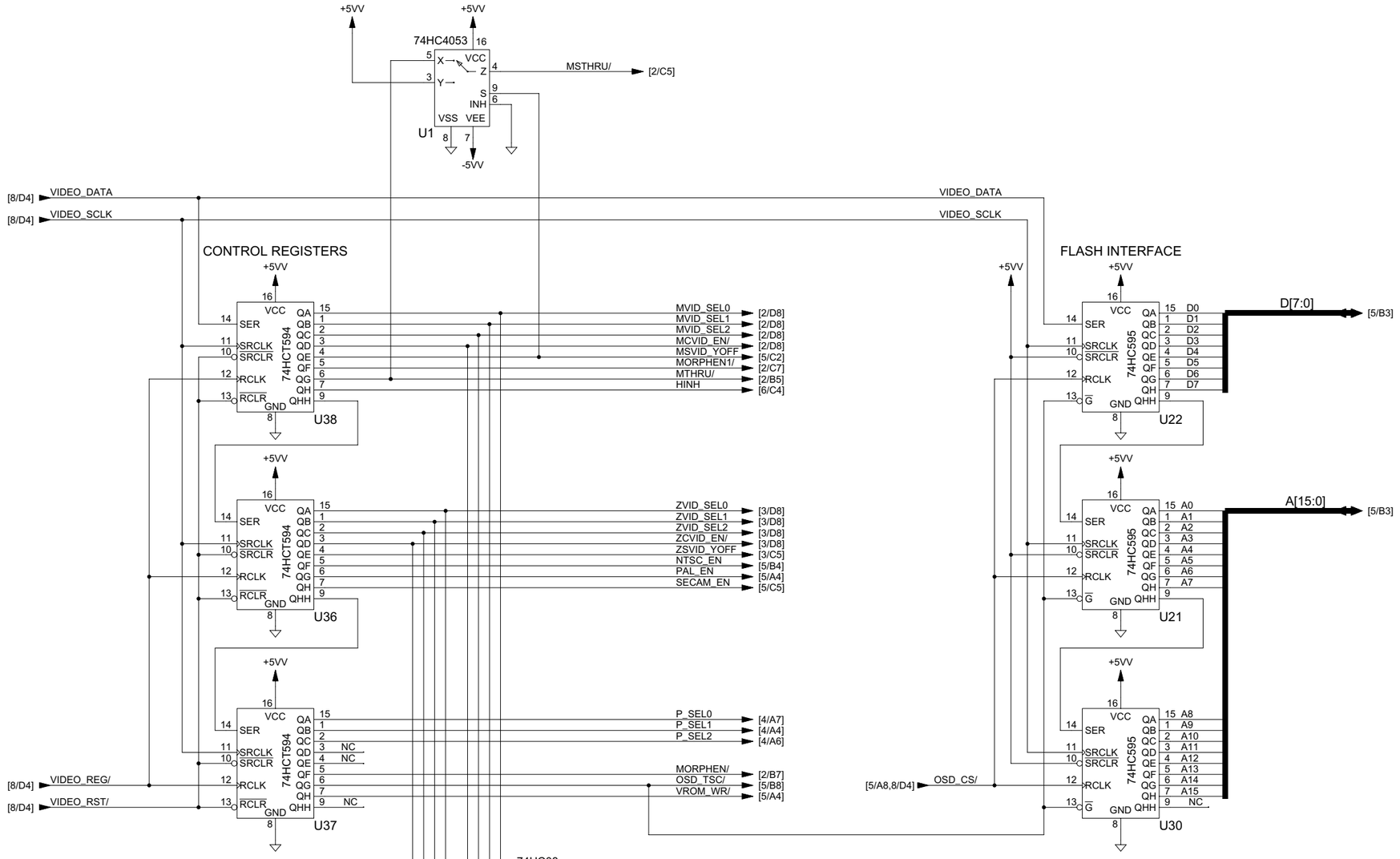
TITLE: SCHEM,VIDEO BD, MC4/MC8
SYNC STRIPPER

SIZE	CODE	NUMBER	REV
B		060-15269	2

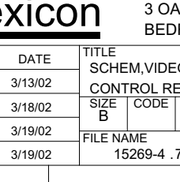
FILE NAME: 15269-4 .6
SHEET 6 OF 8

10-19-2004_8:34

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04



SPARES



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

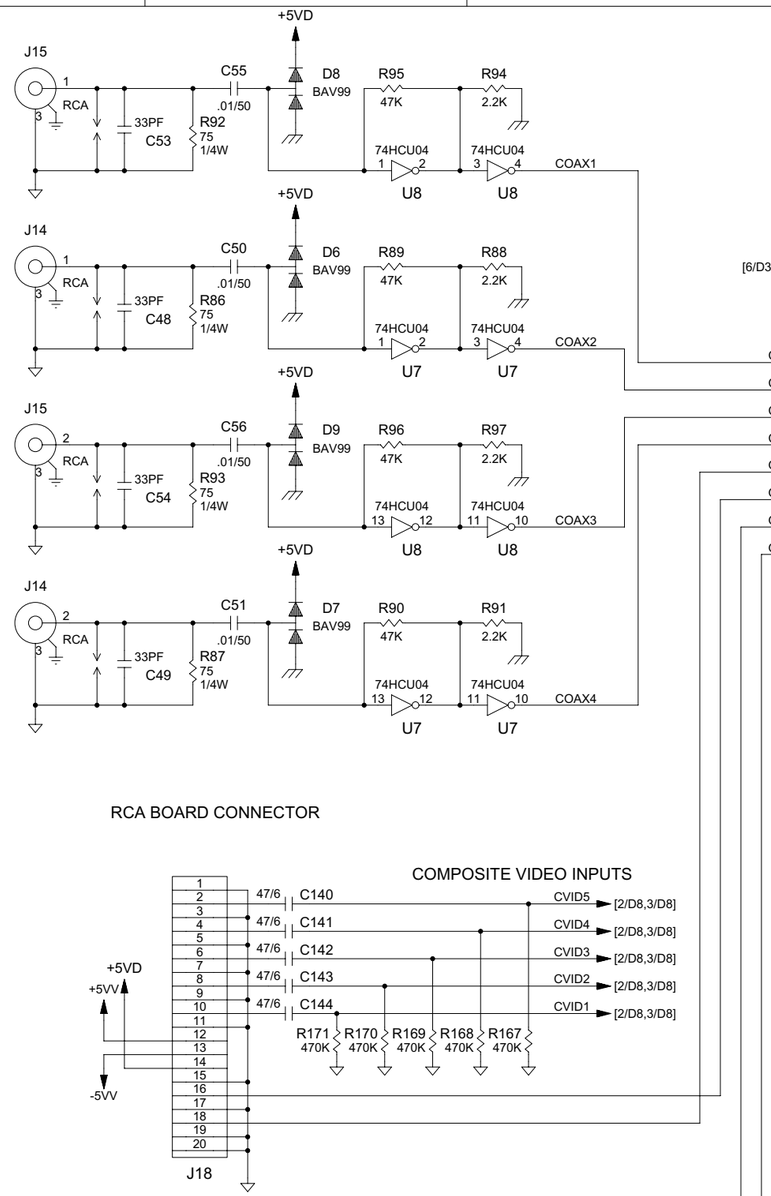
APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

TITLE: SCHEM,VIDEO BD, MC4/MC8
CONTROL REGISTERS

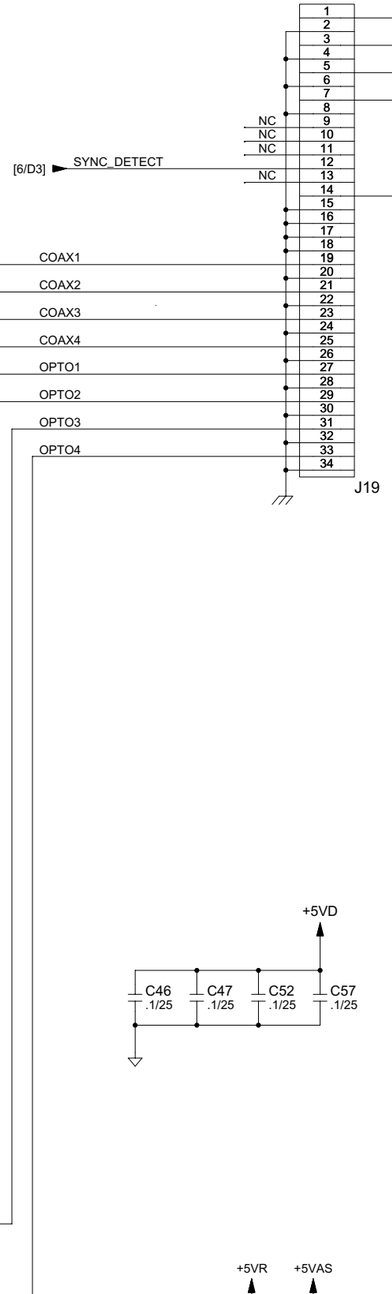
SIZE	CODE	NUMBER	REV
B		060-15269	2

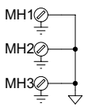
FILE NAME: 15269-4 .7 SHEET 7 OF 8

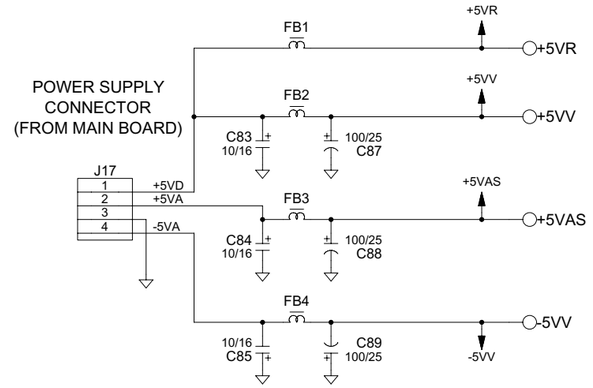
10-19-2004_8:34

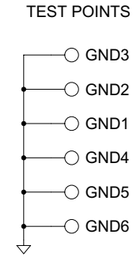


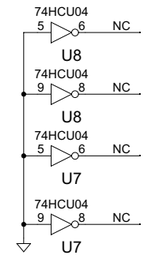
RCA BOARD CONNECTOR

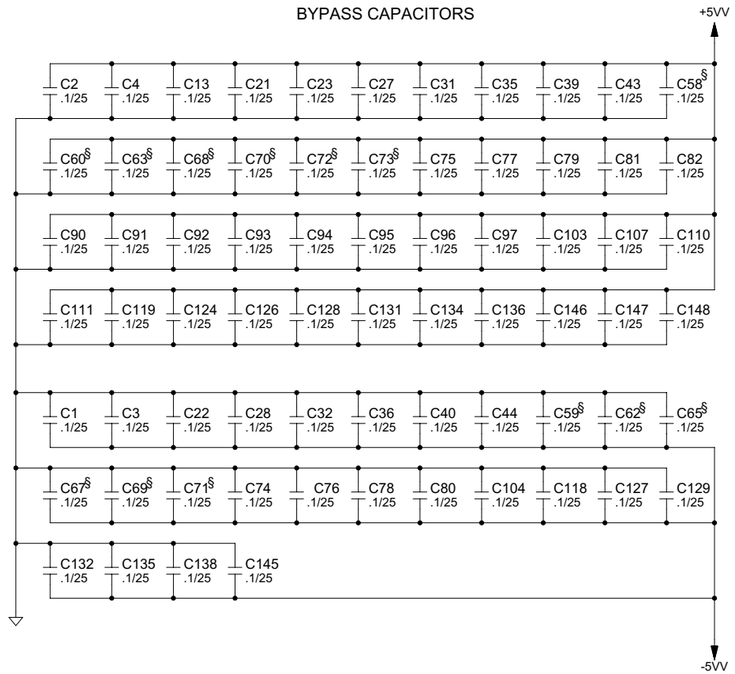


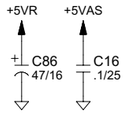


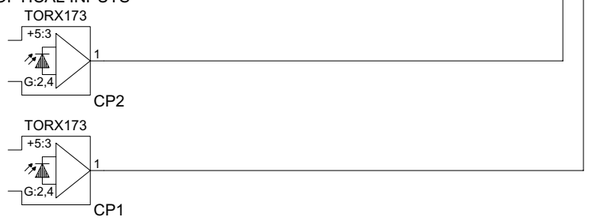












REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020523-00	CW 6/3/02	RWH 6/5/02
		ECM 6/4/02	KAB 6/5/02
2	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/27/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

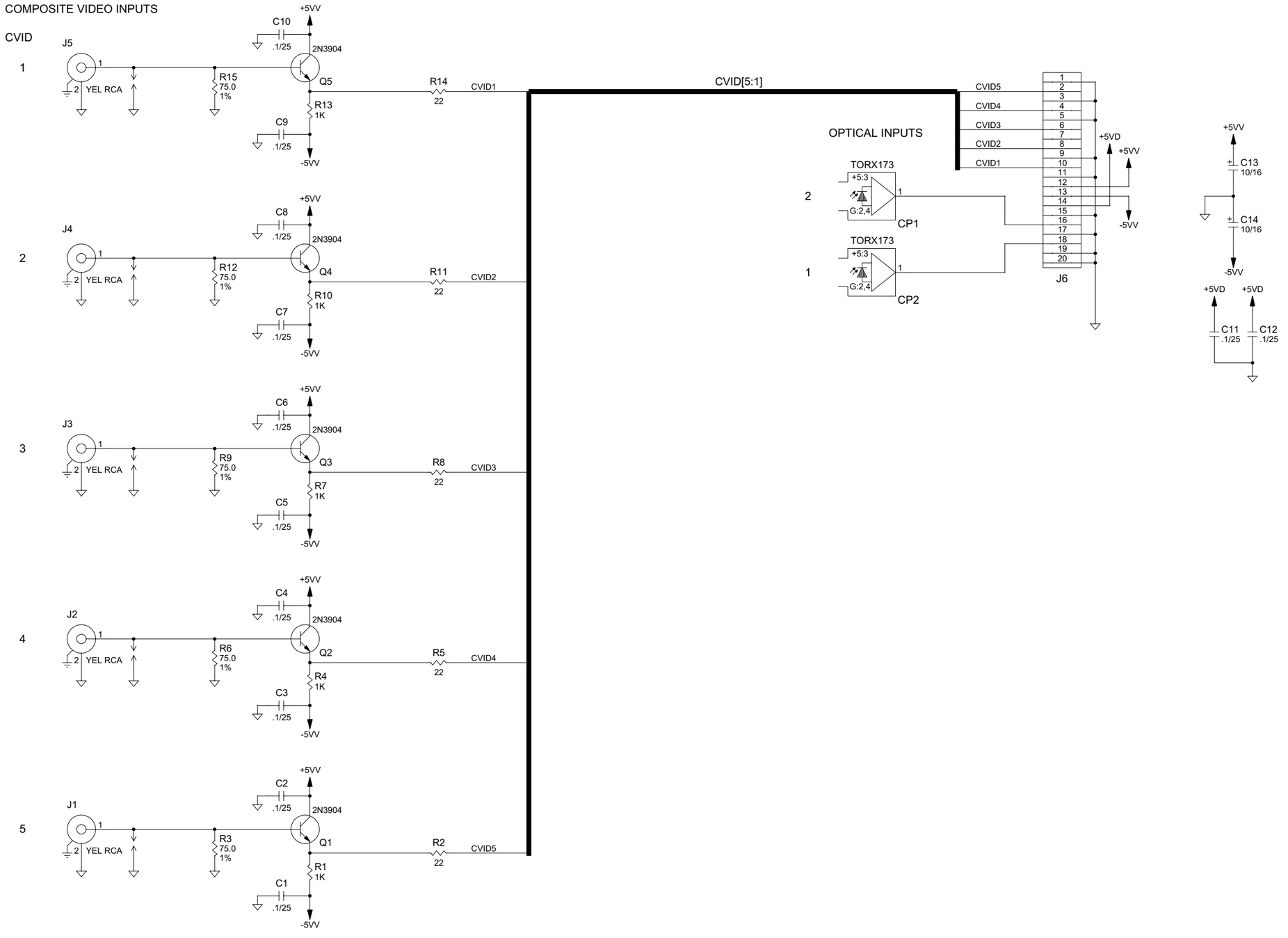
APPROVALS		DATE
DRAWN	RWH	3/13/02
CHECKED	ECM	3/18/02
Q.C.	CW	3/19/02
ISSUED	KB	3/19/02

TITLE: SCHEM,VIDEO BD, MC4/MC8
PWR,SPDIF,MAIN&RCA BD CONNS

SIZE	CODE	NUMBER	REV
B		060-15269	2

FILE NAME: 15269-4 .8
SHEET 8 OF 8

10-21-2004_8:13



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

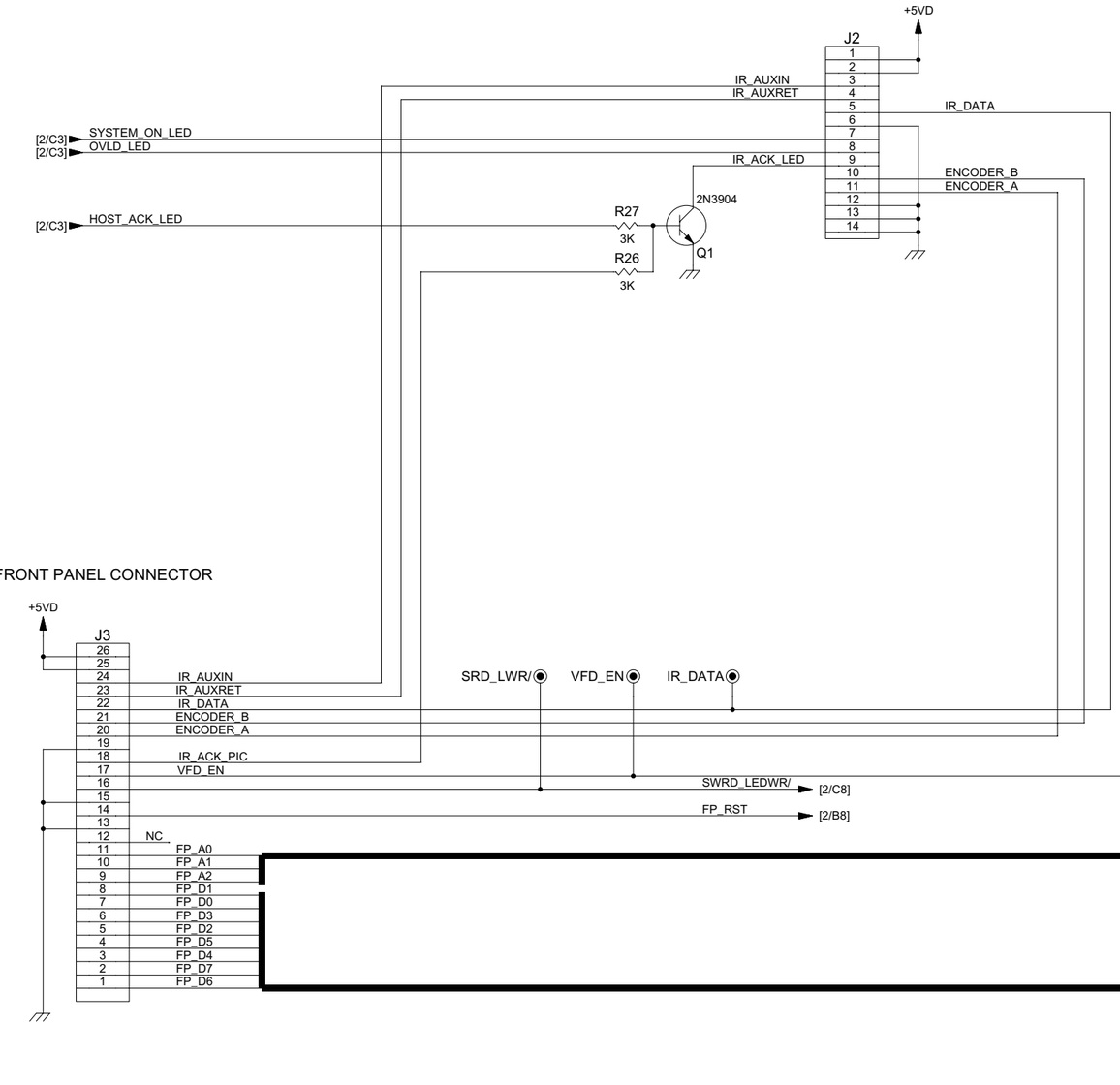
5 LAST REFERENCE DESIGNATORS USED: C14, CP2, J6, Q5, R15

REFERENCE COPY

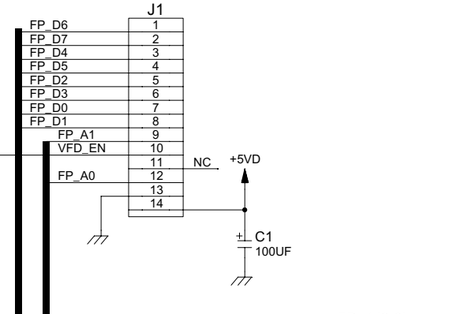
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM,VIDEO RCA BD,MC8 RCA , OPTICAL DIGITAL INPUTS	
DRAWN RWH	1/9/02		
CHECKED ECM	1/10/02	SIZE B / CODE / NUMBER 060-15279 / REV 0	
Q.C. CW	1/10/02		
ISSUED KAB	1/11/02	FILE NAME 15279-0 . 1 / SHEET 1 OF 1	

1-16-2002, 12:16

IR/ENCODER BOARD CONNNECTOR



VFD CONNECTOR



FRONT PANEL CONNECTOR

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, CHASSIS SCREW, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C7, D22, J3, Q1, R29, SW21, U6.

DOCUMENT CONTROL BLOCK: #060-15289

SHEET	REVISION	TITLE
1 OF 3	0	CONNECTORS
2 OF 3	0	CONTROL & STATUS REG
3 OF 3	0	SWITCHES & LEDS

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

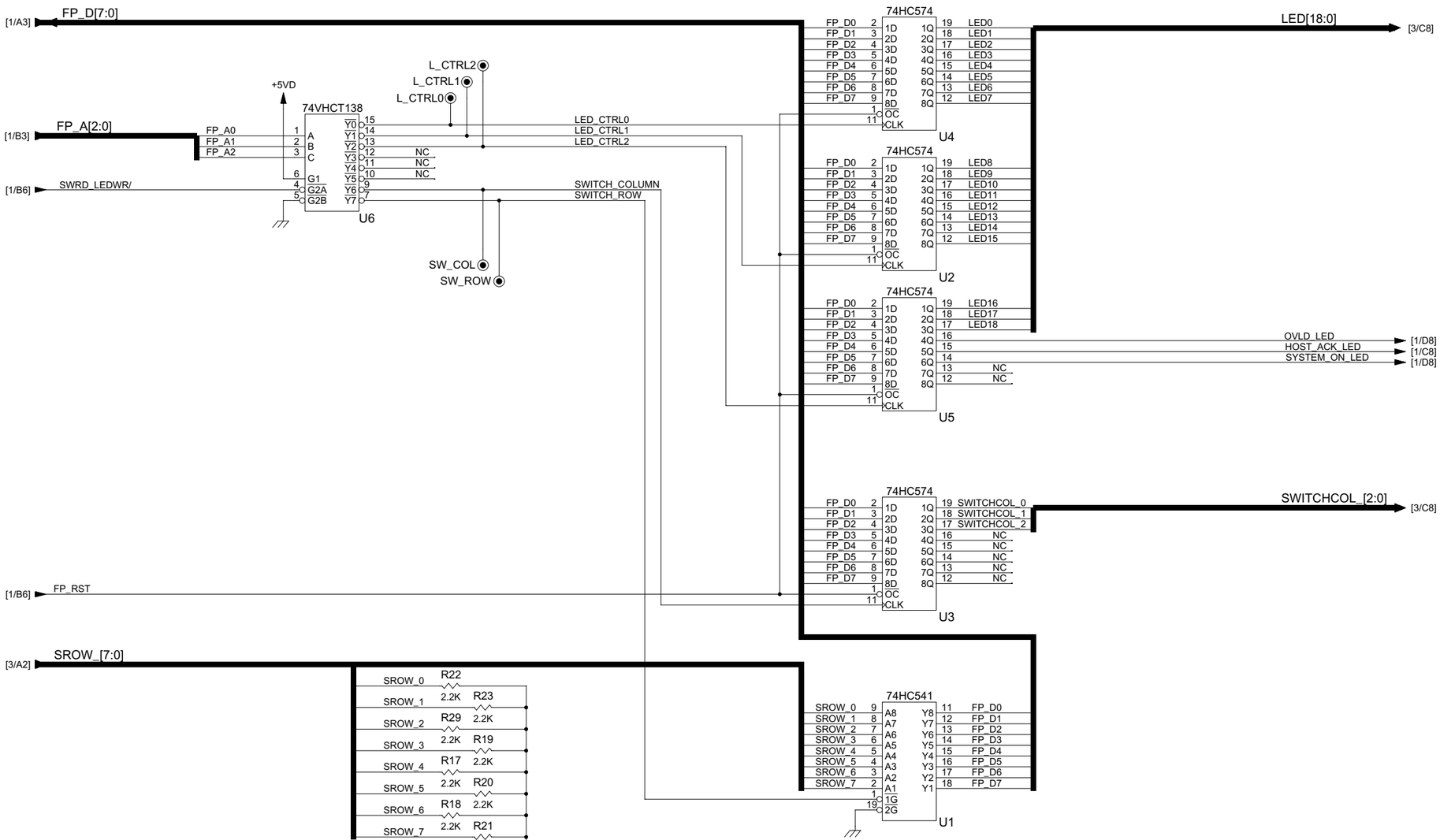
APPROVALS		DATE
DRAWN	RWH	12/21/01
CHECKED	KAB	1/4/02
Q.C.	CW	1/8/02
ISSUED	KAB	1/8/02

TITLE: SCHEM,SW/LED BD,MC8 CONNECTORS

SIZE	CODE	NUMBER	REV
B		060-15289	0

FILE NAME: 15289-0.1 SHEET 1 OF 3

1-16-2002_12:35



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

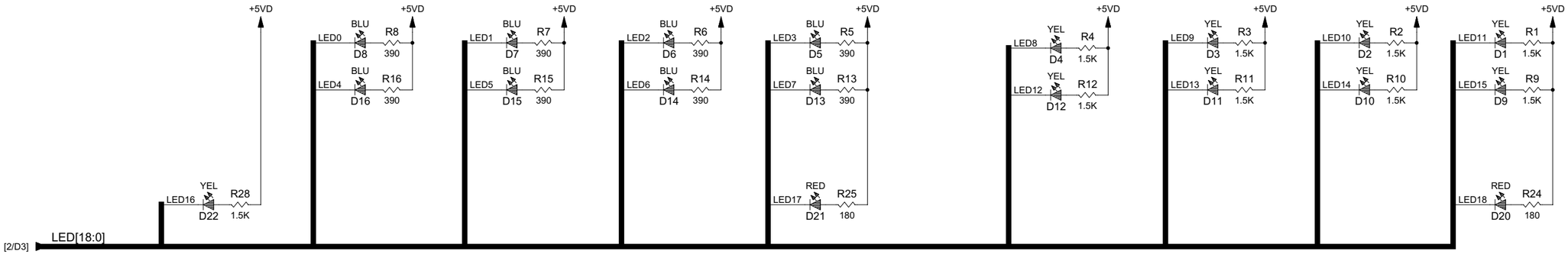
CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730
APPROVALS	DATE	TITLE: SCHEM,SW/LED BD,MC8 CONTROL & STATUS REG
DRAWN RWH	12/21/01	
CHECKED KAB	1/4/02	SIZE B · CODE · NUMBER 060-15289 · REV 0
Q.C. CW	1/8/02	
ISSUED KAB	1/8/02	FILE NAME 15289-0.2 · SHEET 2 OF 3

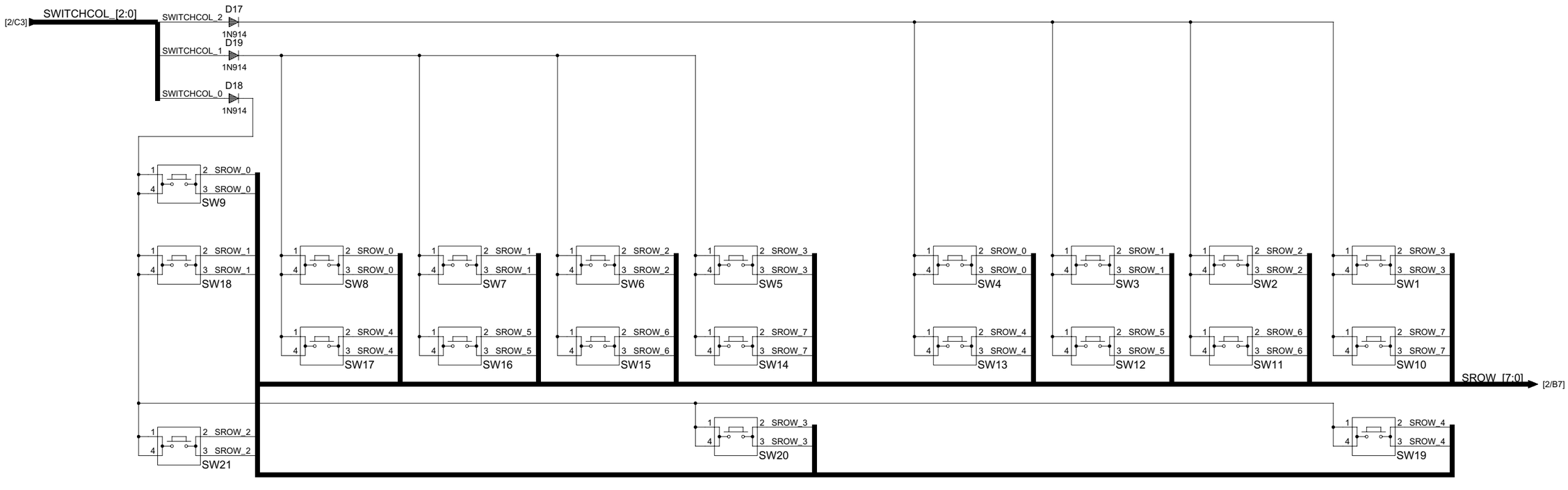
1-16-2002_12:36

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

MAIN

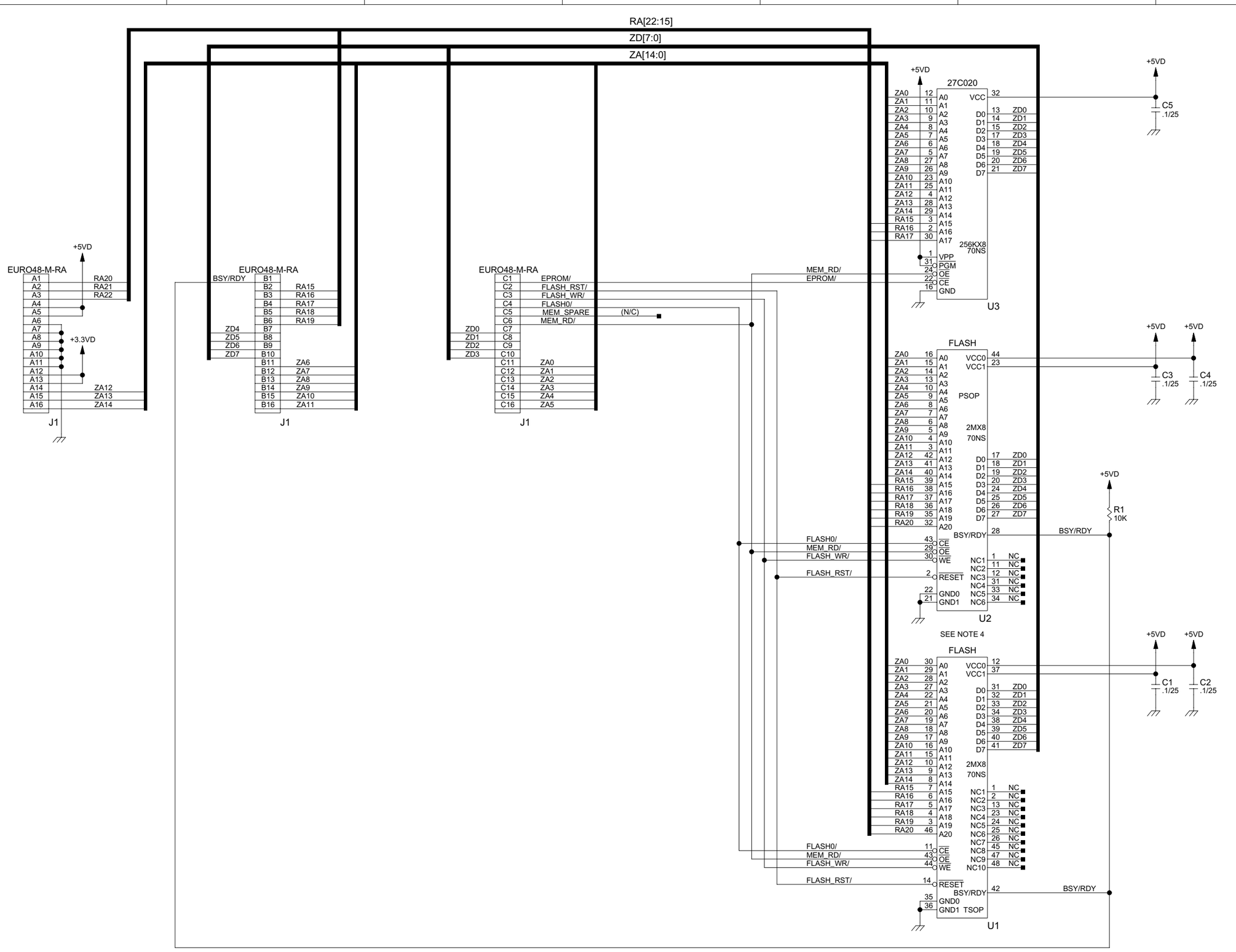
ZONE 2





CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	SCHEM,SW/LED BD,MC8 SWITCHES & LEDS
DRAWN RWH	12/21/01		
CHECKED KAB	1/4/02	SIZE B / CODE / NUMBER 060-15289 / REV 0	
Q.C. CW	1/8/02		
ISSUED KAB	1/8/02	FILE NAME 15289-0.3	SHEET 3 OF 3

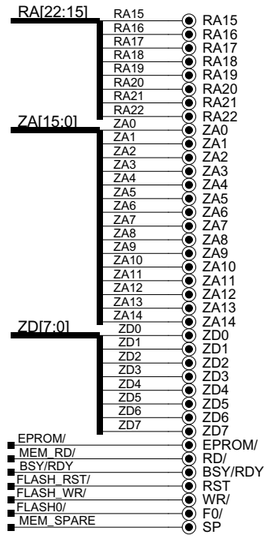
1-16-2002_12:36



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

TEST POINTS



NOTES

1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

2 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

3 LAST REFERENCE DESIGNATORS USED: C5, J1, R1, U3

4 DUAL LAYOUT: INSTALL EITHER U1, C1, C2
OR U2, C3, C4

REFERENCE COPY

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

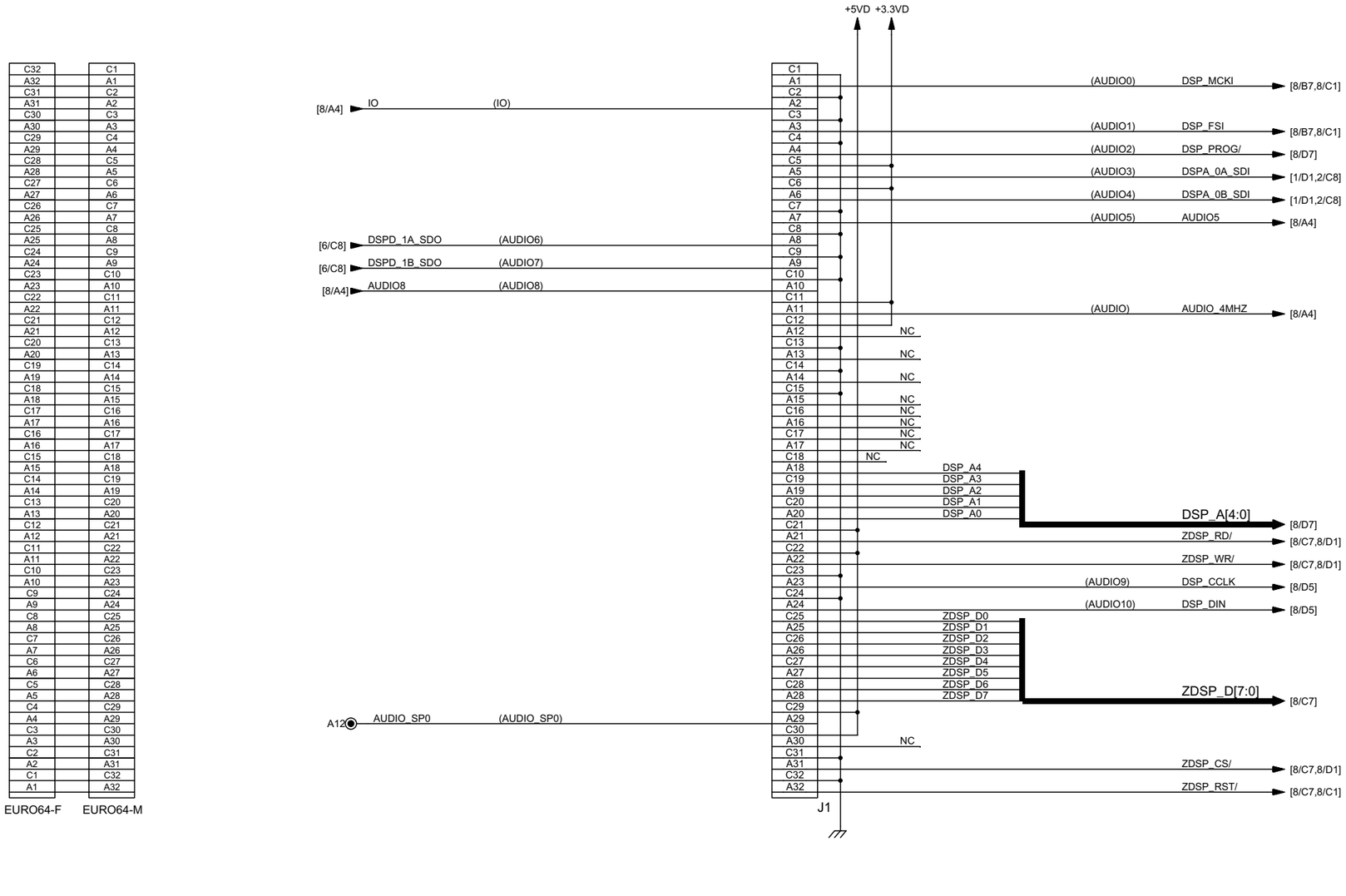
APPROVALS		DATE
DRAWN	RWH	12/6/01
CHECKED	KAB	1/4/02
Q.C.	CW	1/8/02
ISSUED	KAB	1/8/02

TITLE: SCHEM,MEMORY BD,MC8

SIZE	CODE	NUMBER	REV
B		060-15299	0

FILE NAME: 15299-0.1 SHEET 1 OF 1

1-16-2002_12:45



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02
2	UPDATE SIGNAL NAMES ON SHEETS 1,8 PER DCR 020927-00	CW 9/30/02	RWH 10/15/02
		KAB 10/15/02	KAB 10/15/02

TEST POINTS

A0A_SD — DSPA_0A_SDI
A0B_SD — DSPA_0B_SDI

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C98, D9, FB5, J3, Q1, R48, U20, W1

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

8 NAMES IN PARENTHESES DESIGNATE GENERIC NOMENCLATURE USED ON THE MATING CONNECTOR OF THE MAIN BOARD SCHEMATIC.

DOCUMENT CONTROL BLOCK: #060-15309

SHEET	REV	DESCRIPTION
1 OF 9	2	MAIN BD CONNECTOR
2 OF 9	1	DSP A
3 OF 9	1	DSP B
4 OF 9	1	DSPAB EXT MEM
5 OF 9	1	DSP C
6 OF 9	1	DSP D
7 OF 9	1	DSPCD EXT MEM
8 OF 9	2	FPGA
9 OF 9	1	BYPASS CAPACITORS & DSP CLOCKS

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

TITLE
SCHEM,DSP BD,MC8
MAIN BD CONNECTOR

SIZE	CODE	NUMBER	REV
B		060-15309	2

FILE NAME 15309-2.1 SHEET 1 OF 9

11-18-2002 15:51

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

MASTER - ID0 HIGH, ID1 LOW
SLAVE - ID0 LOW, ID1 HIGH

+3.3VD

R45 R46

VCC

ADSP21065

[9/D4]	DSPA_CLK	DSPA_CLK	30	CLKIN	
		NC	31	XTAL2	
[3/C8,8/C4,8/C1]	AB_RST/		152	BSEL	
			157	RESET	
			144	ID0	
			143	ID1	
[3/C8,8/C4,8/C1]	DSPAB_ACK	DSPAB_ACK	69	ACK	
[3/C8,5/C8,6/C8,8/B4,8/C1]	DSP_FSI_IRQ		205	IRQ0	
[3/C8,8/C4]	SP_IRQAB		206	IRQ1	
[8/C4,8/C1]	DSPAB_CMD_RDY/		207	IRQ2	
[3/C6,5/C8,8/B4,8/C1]	DSPABC_FSI		2	RFS0	
[8/B4,8/C1]	DSPA_SCKI		4	RCLK0	
[1/D1,1/C3]	DSPA_0A_SDI		5	DR0A	
[1/D1,1/C3]	DSPA_0B_SDI		6	DR0B	
			7	TFS0	
		NC	8	TCLK0	
		NC	11	DT0A	
		NC	12	DT0B	
			13	RFS1	
		NC	15	RCLK1	
			16	DR1A	
			17	DR1B	
			18	TFS1	
		NC	19	TCLK1	
		NC	22	DT1A	
		NC	23	DT1B	
		NC	26	PWMEVENT0	
		NC	24	PWMEVENT1	
			38	DMAR1	
			39	DMAR2	
			50	DMAG1	
			51	DMAG2	
			40	HBR	
		NC	52	HBG	
			55	CS	
		NC	63	REDY	
			56	SBTS	
[2/C1,3/B8]	DSPAB_CPA/	R42	65	CPA	
[2/C1,3/B8]	DSPAB_BR1/		27	BR1	
[2/C1,3/B8]	DSPAB_BR2/		28	BR2	
		DSPAB_EMU/	145	EMU	
		DSPA_TDO	146	TDO	
		DSPAB_TDI	148	TDI	
		DSPAB_TCK	151	TCK	
		DSPAB_TMS	149	TMS	
		DSPAB_TRST	147	TRST	
[3/B8,8/C4]	DSPAB_STATUS_FULL		197	FLAG0	
[3/B8,5/B8,6/B8,8/B4]	DSP_FLAG1		198	FLAG1	
		NC	199	FLAG2	
			201	FLAG3	AF3
			138	FLAG4	AF4
			137	FLAG5	AF5
			136	FLAG6	AF6
			134	FLAG7	AF7
			80	FLAG8	AF8
			79	FLAG9	
			78	FLAG10	
		NC	76	FLAG11	
		NC	102	NC1	
		NC	103	NC2	
		NC	115	NC3	
		NC	142	NC4	
		NC	202	NC5	
		NC	203	NC6	

		RAS	42	DSPAB_RAS/	[2/D1,3/D3,4/C8]
		CAS	43	DSPAB_CAS/	[2/D1,3/D3,4/C8]
		SDWE	44	DSPAB_SDWE/	[2/D1,3/D3,4/C8]
		DQM	46	DSPAB_DQM	[2/D1,3/D3,4/C8]
		SDCKE	47	DSPAB_SDCKE	[2/D1,3/D3,4/C8]
		SDA10	48	DSPAB_SDA10	[2/D1,3/D3,4/D8]
		SDCLK0	37	DSPAB_SDCLK	[2/D1,3/D3,4/C8]
		SDCLK1	34	NC	
		BMS	153	DSPAB_BMS/	[2/D1,3/C3,8/C7]
		MS0	70	DSPAB_SDRAM_CS	[2/D1,3/C3,4/C8]
		MS1	71	DSPAB_HOST_CS/	[2/D1,3/C3,8/C7]
		MS2	74	DSPAB_SRAM_CS/	[2/D1,3/C3,4/D4]
		MS3	75	NC	
		SW	64	NC	
		WR	58	DSPAB_WR/	[2/D1,3/C3,4/B4]
		RD	59	DSPAB_RD/	[2/D1,3/C3,4/B4]
		A0	195	DSPAB_A0	
		A1	194	DSPAB_A1	
		A2	193	DSPAB_A2	
		A3	190	DSPAB_A3	
		A4	189	DSPAB_A4	
		A5	188	DSPAB_A5	
		A6	185	DSPAB_A6	
		A7	184	DSPAB_A7	
		A8	183	DSPAB_A8	
		A9	180	DSPAB_A9	
		A10	179	DSPAB_A10	
		A11	178	DSPAB_A11	
		A12	175	DSPAB_A12	
		A13	174	DSPAB_A13	
		A14	173	DSPAB_A14	
		A15	171	DSPAB_A15	
		A16	170	DSPAB_A16	
		A17	169	DSPAB_A17	
		A18	166	DSPAB_A18	
		A19	165	DSPAB_A19	
		A20	164	DSPAB_A20	
		A21	162	DSPAB_A21	
		A22	161	DSPAB_A22	
		A23	160	DSPAB_A23	DSPAB_A[23:0] [3/B3,4/D6]
		D0	82	DSPAB_D0	
		D1	83	DSPAB_D1	
		D2	84	DSPAB_D2	
		D3	86	DSPAB_D3	
		D4	87	DSPAB_D4	
		D5	88	DSPAB_D5	
		D6	90	DSPAB_D6	
		D7	91	DSPAB_D7	
		D8	92	DSPAB_D8	
		D9	96	DSPAB_D9	
		D10	97	DSPAB_D10	
		D11	98	DSPAB_D11	
		D12	100	DSPAB_D12	
		D13	101	DSPAB_D13	
		D14	104	DSPAB_D14	
		D15	107	DSPAB_D15	
		D16	108	DSPAB_D16	
		D17	109	DSPAB_D17	
		D18	111	DSPAB_D18	
		D19	112	DSPAB_D19	
		D20	113	DSPAB_D20	
		D21	116	DSPAB_D21	
		D22	117	DSPAB_D22	
		D23	118	DSPAB_D23	
		D24	121	DSPAB_D24	
		D25	122	DSPAB_D25	
		D26	123	DSPAB_D26	
		D27	126	DSPAB_D27	
		D28	127	DSPAB_D28	
		D29	128	DSPAB_D29	
		D30	132	DSPAB_D30	
		D31	133	DSPAB_D31	DSPAB_D[31:0] [3/A3,4/D7,8/C4]
		BMSTR	53	DSPA_BMSTR	DSPA_BMSTR
		NC7	208	NC	

GND

U16

DEVELOPMENT ONLY:
PIN 7, BTCK, JUMP TO PIN 8
PIN 9, BTRST/, JUMP TO PIN 10

+3.3VD +3.3VD

R48 R47

	1	2	DSPAB_EMU/	DSPA_TDO [3/B8] DSPAB_EMU/ [3/B8]
NC	3	4	DSPAB_ICE_CLK	
NC	5	6	DSPAB_TMS	DSPAB_TMS [3/B8]
	7	8	DSPAB_TCK	DSPAB_TCK [3/B8]
	9	10	DSPAB_TRST	DSPAB_TRST [3/B8]
NC	11	12	DSPAB_TDI	
	13	14		

* J3

[3/B8] DSPB_TDO
[2/D1,9/C4] DSPAB_ICE_CLK

DSPA_OUT1 [4/B8,8/C7]
DSPA_OUT0 [4/B8,8/C7]

TEST POINTS

ABCLK	DSPAB_ICE_CLK
ABWR	DSPAB_WR/
ABRD	DSPAB_RD/
ABBMS	DSPAB_BMS/
ABHOST_CS	DSPAB_HOST_CS/
ABSRAM_CS	DSPAB_SRAM_CS/
ABSDRAM_CS	DSPAB_SDRAM_CS/
ABRAS	DSPAB_RAS/
ABCAS	DSPAB_CAS/
ABSDWE	DSPAB_SDWE/
ABDQM	DSPAB_DQM
ABSDCKE	DSPAB_SDCKE
ABSDA10	DSPAB_SDA10
ABSDCLK	DSPAB_SDCLK
ABCPA	DSPAB_CPA/
ABBR1	DSPAB_BR1/
ABBR2	DSPAB_BR2/

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,DSP BD,MC8 DSP A
DRAWN	RWH	2/28/02	
CHECKED	KB	3/5/02	SIZE: B; CODE: ; NUMBER: 060-15309; REV: 1
Q.C.	CW	3/5/02	
ISSUED	KB	3/5/02	FILE NAME: 15309-2.2; SHEET: 2 OF 9

11-18-2002_15:51

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

MASTER - ID0 HIGH, ID1 LOW
SLAVE - ID0 LOW, ID1 HIGH

+3.3VD

R44 R43

VCC

ADSP21065

[9/D4]	DSPB_CLK	30	CLKIN
		NC 31	XTAL2
		152	BSEL
[2/C8,8/C4,8/C1]	AB_RST/	157	RESET
		144	ID0
		143	ID1
[2/C8,8/C4,8/C1]	DSPAB_ACK	69	ACK
[2/C8,5/C8,6/C8,8/B4,8/C1]	DSP_FSI_IRQ	205	IRQ0
[2/C8,8/C4]	SP_IRQAB	206	IRQ1
		207	IRQ2
		2	RFS0
		NC 4	RCLK0
		5	DR0A
		6	DR0B
[2/C8,5/C8,8/B4,8/C1]	DSPABC_FSI	7	TFS0
[8/A4]	DSPB_SCKI	8	TCLK0
		NC 11	DT0A
		NC 12	DT0B
		13	RFS1
		NC 15	RCLK1
		16	DR1A
		17	DR1B
		18	TFS1
		19	TCLK1
[3/D1,5/C8]	DSPB_1A_SDO	22	DT1A
[3/D1,5/C8]	DSPB_1B_SDO	23	DT1B
		NC 26	PWMEVENT0
		NC 24	PWMEVENT1
		38	DMAR1
		39	DMAR2
		50	DMAG1
		51	DMAG2
		40	HBR
		NC 52	HBG
		55	CS
		NC 63	REDY
		56	SBTS
[2/C1,2/B8]	DSPAB_CPA/	65	CPA
[2/C1,2/B8]	DSPAB_BR1/	27	BR1
[2/C1,2/B8]	DSPAB_BR2/	28	BR2
[2/A6]	DSPAB_EMU/	145	EMU
[2/A8]	DSPB_TDO	146	TDO
[2/A6]	DSPA_TDO	148	TDI
[2/A6]	DSPAB_TCK	151	TCK
[2/A6]	DSPAB_TMS	149	TMS
[2/A6]	DSPAB_TRST	147	TRST
[2/B8,8/C4]	DSPAB_STATUS_FULL	197	FLAG0
[2/B8,5/B8,6/B8,8/B4]	DSP_FLAG1	198	FLAG1
		NC 199	FLAG2
BF3		201	FLAG3
BF4		138	FLAG4
BF5		137	FLAG5
BF6		136	FLAG6
BF7		134	FLAG7
BF8		80	FLAG8
		79	FLAG9
		78	FLAG10
		NC 76	FLAG11
		NC 102	NC1
		NC 103	NC2
		NC 115	NC3
		NC 142	NC4
		NC 202	NC5
		NC 203	NC6

GND

U15

		42	RAS
		43	CAS
		44	SDWE
		46	DQM
		47	SDCKE
		48	SDA10
		37	SDCLK0
		34 NC	SDCLK1
		153	BMS
		70	MS0
		71	MS1
		74	MS2
		75 NC	MS3
		64 NC	SW
		58	WR
		59	RD
		195	A0
		194	A1
		193	A2
		190	A3
		189	A4
		188	A5
		185	A6
		184	A7
		183	A8
		180	A9
		179	A10
		178	A11
		175	A12
		174	A13
		173	A14
		171	A15
		170	A16
		169	A17
		166	A18
		165	A19
		164	A20
		162	A21
		161	A22
		160	A23
		82	D0
		83	D1
		84	D2
		86	D3
		87	D4
		88	D5
		90	D6
		91	D7
		92	D8
		96	D9
		97	D10
		98	D11
		100	D12
		101	D13
		104	D14
		107	D15
		108	D16
		109	D17
		111	D18
		112	D19
		113	D20
		116	D21
		117	D22
		118	D23
		121	D24
		122	D25
		123	D26
		126	D27
		127	D28
		128	D29
		132	D30
		133	D31
BMSTR		53	DSPB_BMSTR
NC7		208 NC	

DSPAB_RAS/	[2/D1,2/D3,4/C8]
DSPAB_CAS/	[2/D1,2/D3,4/C8]
DSPAB_SDWE/	[2/D1,2/D3,4/C8]
DSPAB_DQM	[2/D1,2/D3,4/C8]
DSPAB_SDCKE	[2/D1,2/D3,4/C8]
DSPAB_SDA10	[2/D1,2/D3,4/D8]
DSPAB_SDCLK	[2/D1,2/D3,4/C8]
DSPAB_BMS/	[2/D1,2/C3,8/C7]
DSPAB_SDRAM_CS/	[2/D1,2/C3,4/C8]
DSPAB_HOST_CS/	[2/D1,2/C3,8/C7]
DSPAB_SRAM_CS/	[2/D1,2/C3,4/D4]
DSPAB_WR/	[2/D1,2/C3,4/B4]
DSPAB_RD/	[2/D1,2/C3,4/B4]

FB5 DSPAB_WR_X/ [8/C7]

FB4 DSPAB_RD_X/ [8/C7]

DSPAB_A[23:0] [2/B3,4/D6]

DSPAB_D[31:0] [2/A3,4/D7,8/C4]

DSPB_BMSTR DSPB_BMSTR

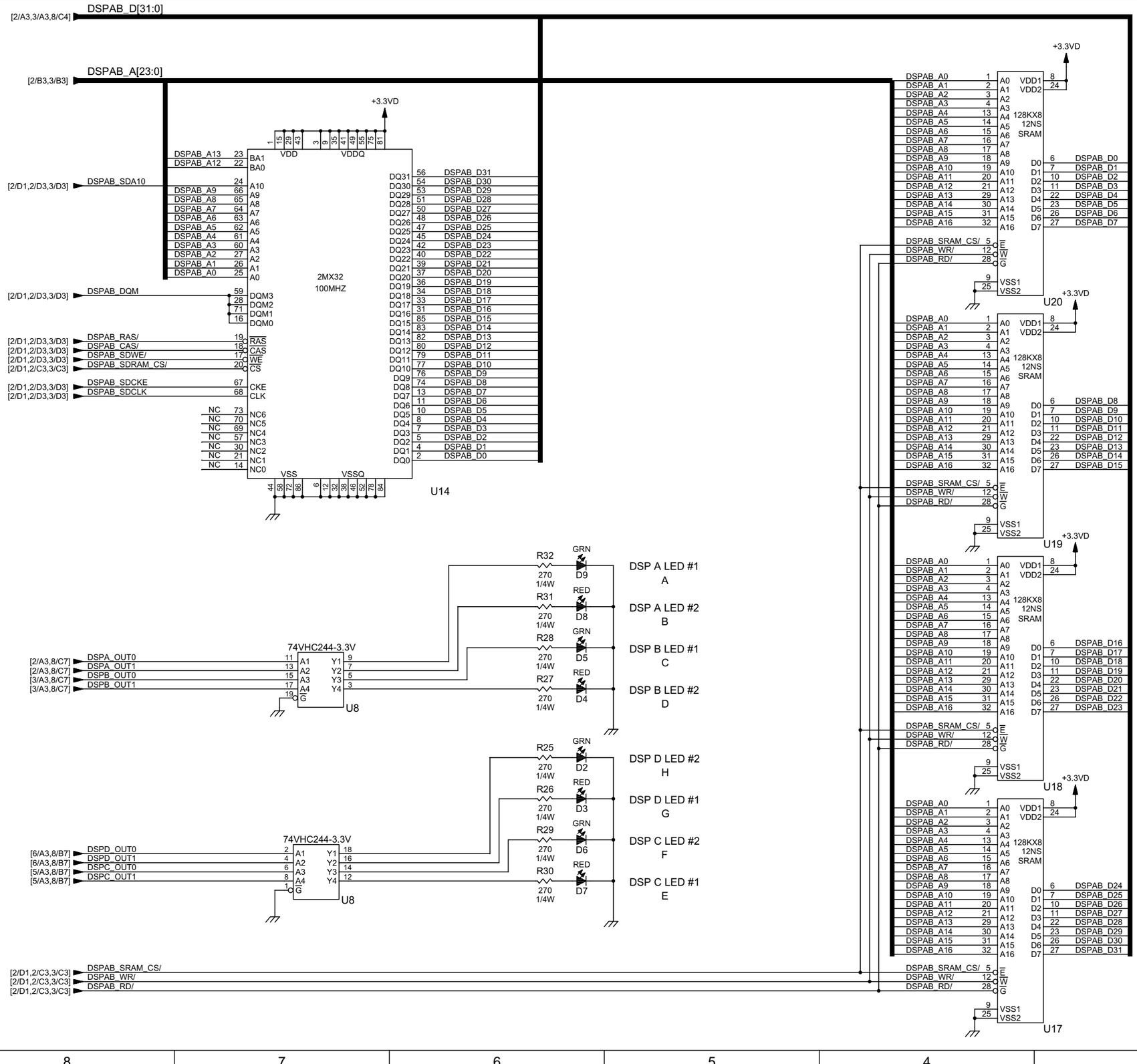
DSPB_OUT1	[4/B8,8/C7]
DSPB_OUT0	[4/B8,8/C7]

TEST POINTS

B1A_SDO DSPB_1A_SDO
B1B_SDO DSPB_1B_SDO

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE SCHEM,DSP BD,MC8 DSP B
DRAWN	RWH	2/28/02	
CHECKED	KB	3/5/02	SIZE B / CODE / NUMBER 060-15309 / REV 1
Q.C.	CW	3/5/02	
ISSUED	KB	3/5/02	FILE NAME 15309-2.3 / SHEET 3 OF 9

11-18-2002_15:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

TITLE
SCHEM,DSP BD,MC8
DSPAB EXT MEM

SIZE	CODE	NUMBER	REV
B		060-15309	1

FILE NAME 15309-2.4 SHEET 4 OF 9

11-18-2002_15:51

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

+3.3VD

MASTER - ID0 HIGH, ID1 LOW
SLAVE - ID0 LOW, ID1 HIGH

R21 R22

VCC

ADSP21065

[9/C4] DSPC_CLK — DSPC_CLK — 30 CLKIN
NC — 31 XTAL2
152 BSEL
[6/D8,8/B4,8/C1] CD_RST/ — 157 RESET
144 ID0
143 ID1
[6/D8,8/B4,8/C1] DSPCD_ACK — DSPCD_ACK — 69 ACK

[2/C8,3/C8,6/C8,8/B4,8/C1] DSP_FSI_IRQ — 205 IRQ0
[6/C8,8/B4] SP_IRQCD — 206 IRQ1
[8/B4,8/C1] DSPCD_CMD_RDY/ — 207 IRQ2

[2/C8,3/C6,8/B4,8/C1] DSPABC_FSI — 2 RFS0
[8/A4,8/C1] DSPC_SCKI — 4 RCLK0
[3/D1,3/C8] DSPB_1A_SDO — 5 DR0A
[3/D1,3/C8] DSPB_1B_SDO — 6 DR0B
7 TFS0
NC — 8 TCLK0
NC — 11 DT0A
NC — 12 DT0B
13 RFS1
NC — 15 RCLK1
16 DR1A
17 DR1B
18 TFS1
NC — 19 TCLK1
NC — 22 DT1A
NC — 23 DT1B
NC — 26 PWMEVENT0
NC — 24 PWMEVENT1
38 DMAR1
39 DMAR2
50 DMAG1
51 DMAG2
40 HBR
NC — 52 HBG
55 CS
NC — 63 REDY
56 SBTS

[5/C1,6/B8] DSPCD_CPA/ — R20 — 65 CPA
[5/C1,6/B8] DSPCD_BR1/ — 27 BR1
[5/C1,6/B8] DSPCD_BR2/ — 28 BR2

DSPCD_EMU/ — 145 EMU
DSPC_TDO — 146 TDO
DSPCD_TDI — 148 TDI
DSPCD_TCK — 151 TCK
DSPCD_TMS — 149 TMS
DSPCD_TRST — 147 TRST

[6/B8,8/B4] DSPCD_STATUS_FULL — 197 FLAG0
[2/B8,3/B8,6/B8,8/B4] DSP_FLAG1 — 198 FLAG1
NC — 199 FLAG2
201 FLAG3
CF3 — 138 FLAG4
CF4 — 137 FLAG5
CF5 — 136 FLAG6
CF6 — 134 FLAG7
CF7 — 80 FLAG8
CF8 — 79 FLAG9
78 FLAG10
NC — 76 FLAG11

NC — 102 NC1
NC — 103 NC2
NC — 115 NC3
NC — 142 NC4
NC — 202 NC5
NC — 203 NC6

GND

U6

DEVELOPMENT ONLY:

PIN 7, BTCK, JUMP TO PIN 8
PIN 9, BTRST/, JUMP TO PIN 10

+3.3VD +3.3VD

R24

1 2 DSPCD_EMU/ — DSPC_TDO / DSPCD_EMU/ — [6/B8] [6/B8]
NC — 3 4 DSPCD_ICE_CLK
NC — 5 6 DSPCD_TMS — DSPCD_TMS — [6/B8]
7 8 DSPCD_TCK — DSPCD_TCK — [6/B8]
9 10 DSPCD_TRST — DSPCD_TRST — [6/B8]
NC — 11 12 DSPCD_TDI
13 14

* J2

R23

[6/B8] DSPD_TDO
[5/D1,9/C4] DSPCD_ICE_CLK

RAS — 42 — DSPCD_RAS/ — [5/C1,6/D3,7/C8]
CAS — 43 — DSPCD_CAS/ — [5/C1,6/D3,7/C8]
SDWE — 44 — DSPCD_SDWE/ — [5/C1,6/D3,7/C8]
DQM — 46 — DSPCD_DQM — [5/C1,6/D3,7/C8]
SDCKE — 47 — DSPCD_SDCKE — [5/C1,6/D3,7/C8]
SDA10 — 48 — DSPCD_SDA10 — [5/C1,6/D3,7/D8]
SDCLK0 — 37 — DSPCD_SDCLK — [5/C1,6/D3,7/C8]
SDCLK1 — 34 NC

BMS — 153 — DSPCD_BMS/ — [5/D1,6/D3,8/B7]
MS0 — 70 — DSPCD_SDRAM_CS/ — [5/C1,6/D3,7/C8]
MS1 — 71 — DSPCD_HOST_CS/ — [5/C1,6/D3,8/B7]
MS2 — 74 — DSPCD_SRAM_CS/ — [5/C1,6/C3,7/D4]
MS3 — 75 NC
SW — 64 NC
WR — 58 — DSPCD_WR/ — [5/D1,6/C3,7/B4]
RD — 59 — DSPCD_RD/ — [5/D1,6/C3,7/B4]

A0 — 195 DSPCD_A0
A1 — 194 DSPCD_A1
A2 — 193 DSPCD_A2
A3 — 190 DSPCD_A3
A4 — 189 DSPCD_A4
A5 — 188 DSPCD_A5
A6 — 185 DSPCD_A6
A7 — 184 DSPCD_A7
A8 — 183 DSPCD_A8
A9 — 180 DSPCD_A9
A10 — 179 DSPCD_A10
A11 — 178 DSPCD_A11
A12 — 175 DSPCD_A12
A13 — 174 DSPCD_A13
A14 — 173 DSPCD_A14
A15 — 171 DSPCD_A15
A16 — 170 DSPCD_A16
A17 — 169 DSPCD_A17
A18 — 166 DSPCD_A18
A19 — 165 DSPCD_A19
A20 — 164 DSPCD_A20
A21 — 162 DSPCD_A21
A22 — 161 DSPCD_A22
A23 — 160 DSPCD_A23

FB2 — DSPCD_WR_X/ — [8/B7]
FB3 — DSPCD_RD_X/ — [8/B7]

DSPCD_A[23:0] — [6/C3,7/D5]

D0 — 82 DSPCD_D0
D1 — 83 DSPCD_D1
D2 — 84 DSPCD_D2
D3 — 86 DSPCD_D3
D4 — 87 DSPCD_D4
D5 — 88 DSPCD_D5
D6 — 90 DSPCD_D6
D7 — 91 DSPCD_D7
D8 — 92 DSPCD_D8
D9 — 96 DSPCD_D9
D10 — 97 DSPCD_D10
D11 — 98 DSPCD_D11
D12 — 100 DSPCD_D12
D13 — 101 DSPCD_D13
D14 — 104 DSPCD_D14
D15 — 107 DSPCD_D15
D16 — 108 DSPCD_D16
D17 — 109 DSPCD_D17
D18 — 111 DSPCD_D18
D19 — 112 DSPCD_D19
D20 — 113 DSPCD_D20
D21 — 116 DSPCD_D21
D22 — 117 DSPCD_D22
D23 — 118 DSPCD_D23
D24 — 121 DSPCD_D24
D25 — 122 DSPCD_D25
D26 — 123 DSPCD_D26
D27 — 126 DSPCD_D27
D28 — 127 DSPCD_D28
D29 — 128 DSPCD_D29
D30 — 132 DSPCD_D30
D31 — 133 DSPCD_D31

DSPCD_D[31:0] — [6/A3,7/D7,8/B4]

BMSTR — 53 DSPC_BMSTR — DSPC_BMSTR
NC7 — 208 NC

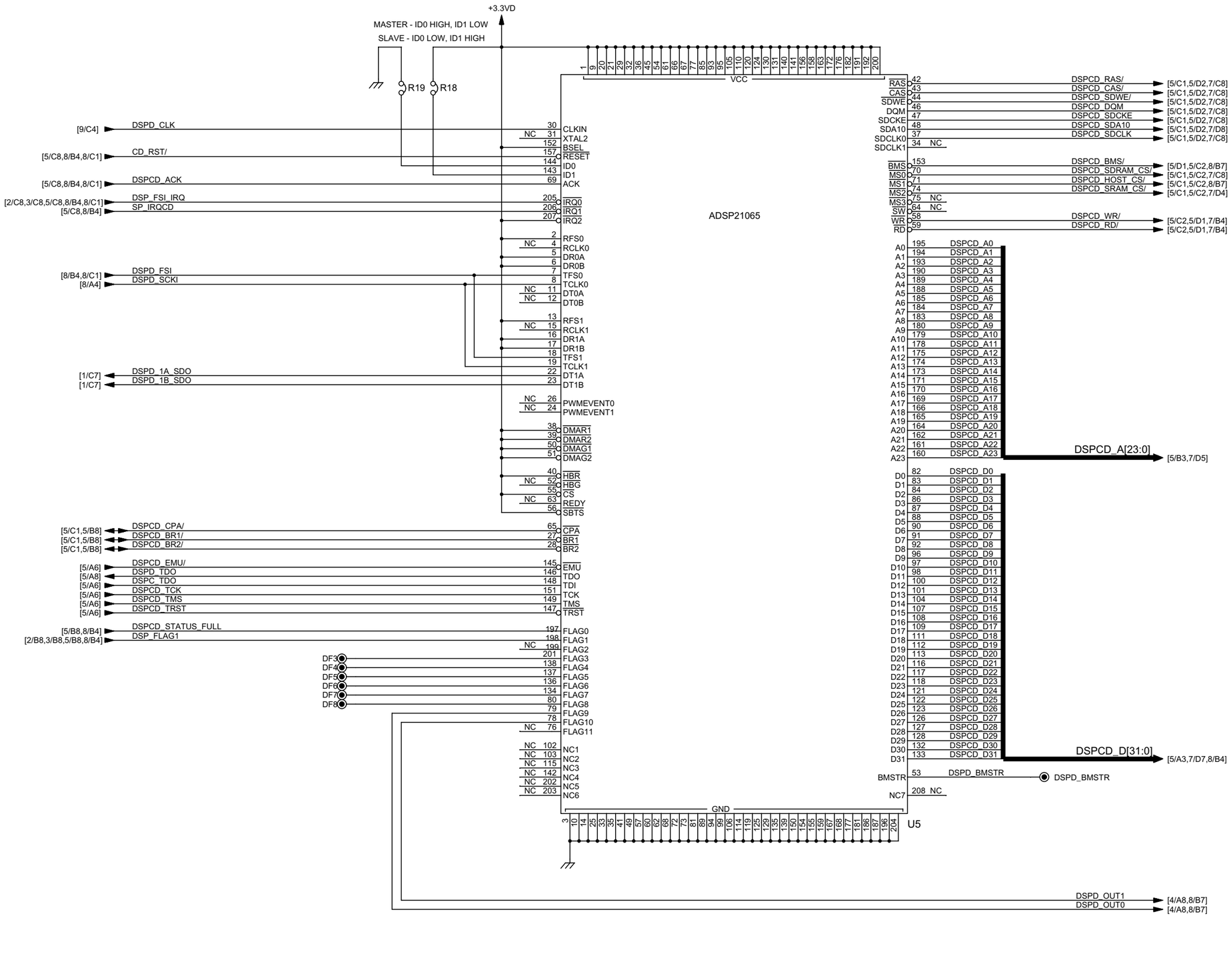
DSPC_OUT1 — [4/A8,8/B7]
DSPC_OUT0 — [4/A8,8/B7]

TEST POINTS

CDCLK — DSPCD_ICE_CLK
CDWR — DSPCD_WR/
CDRD — DSPCD_RD/
CDBMS — DSPCD_BMS/
CDHOST_CS — DSPCD_HOST_CS/
CDSRAM_CS — DSPCD_SRAM_CS/
CDSDRAM_CS — DSPCD_SDRAM_CS/
CDRAS — DSPCD_RAS/
CDCAS — DSPCD_CAS/
CDSDWE — DSPCD_SDWE/
CDDQM — DSPCD_DQM
CDDCKE — DSPCD_SDCKE
CDSDA10 — DSPCD_SDA10
CDSDCLK — DSPCD_SDCLK
CDCPA — DSPCD_CPA/
CDBR1 — DSPCD_BR1/
CDBR2 — DSPCD_BR2/

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	SCHEM,DSP BD,MC8 DSP C
DRAWN RWH	2/28/02		
CHECKED KB	3/5/02	SIZE B	CODE NUMBER 060-15309 REV 1
Q.C. CW	3/5/02		
ISSUED KB	3/5/02	FILE NAME 15309-2.5	SHEET 5 OF 9

11-18-2002_15:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

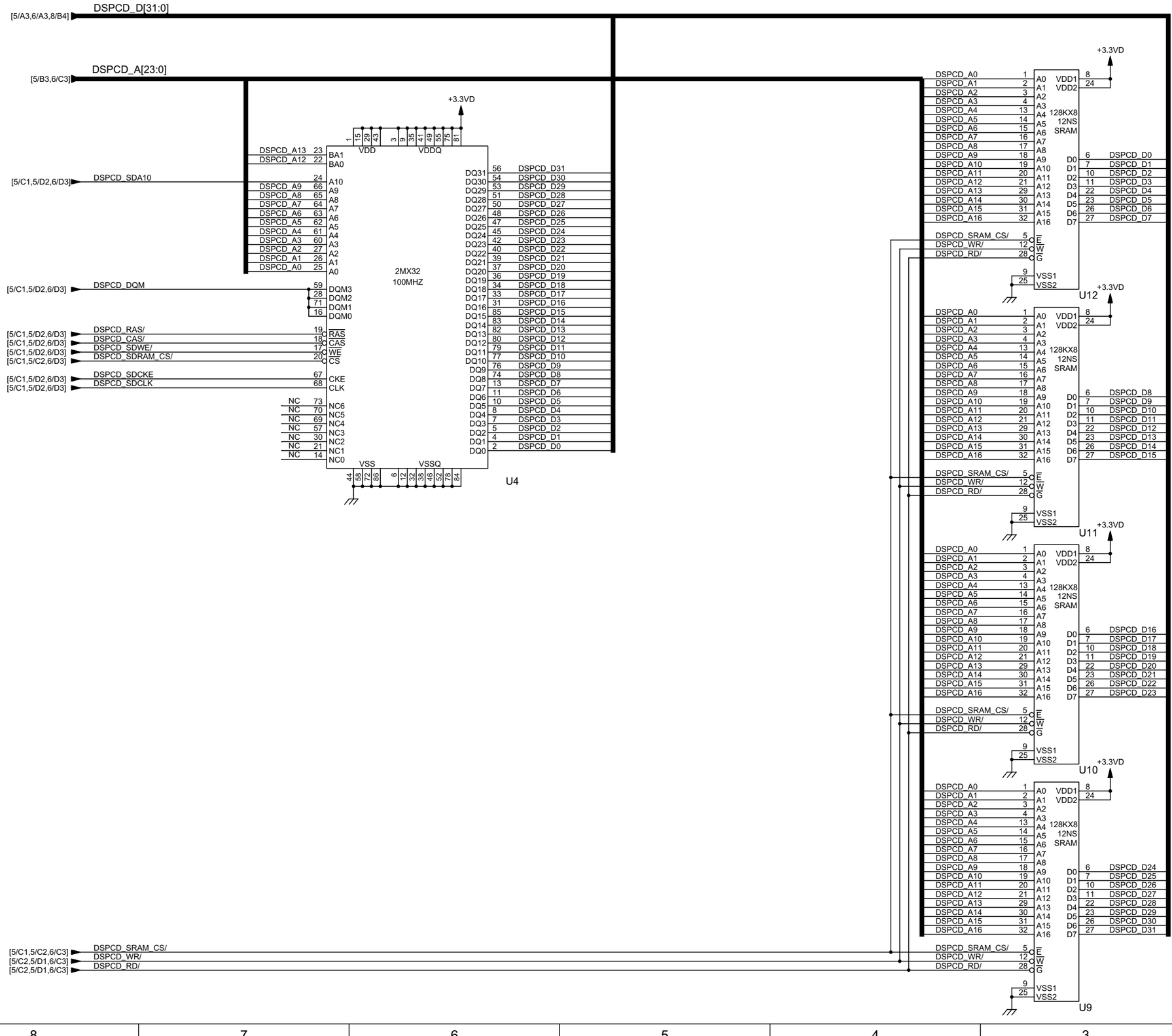
APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

TITLE: SCHEM,DSP BD,MC8
DSP D

SIZE	CODE	NUMBER	REV
B		060-15309	1

FILE NAME: 15309-2.6
SHEET 6 OF 9

11-18-2002 15:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

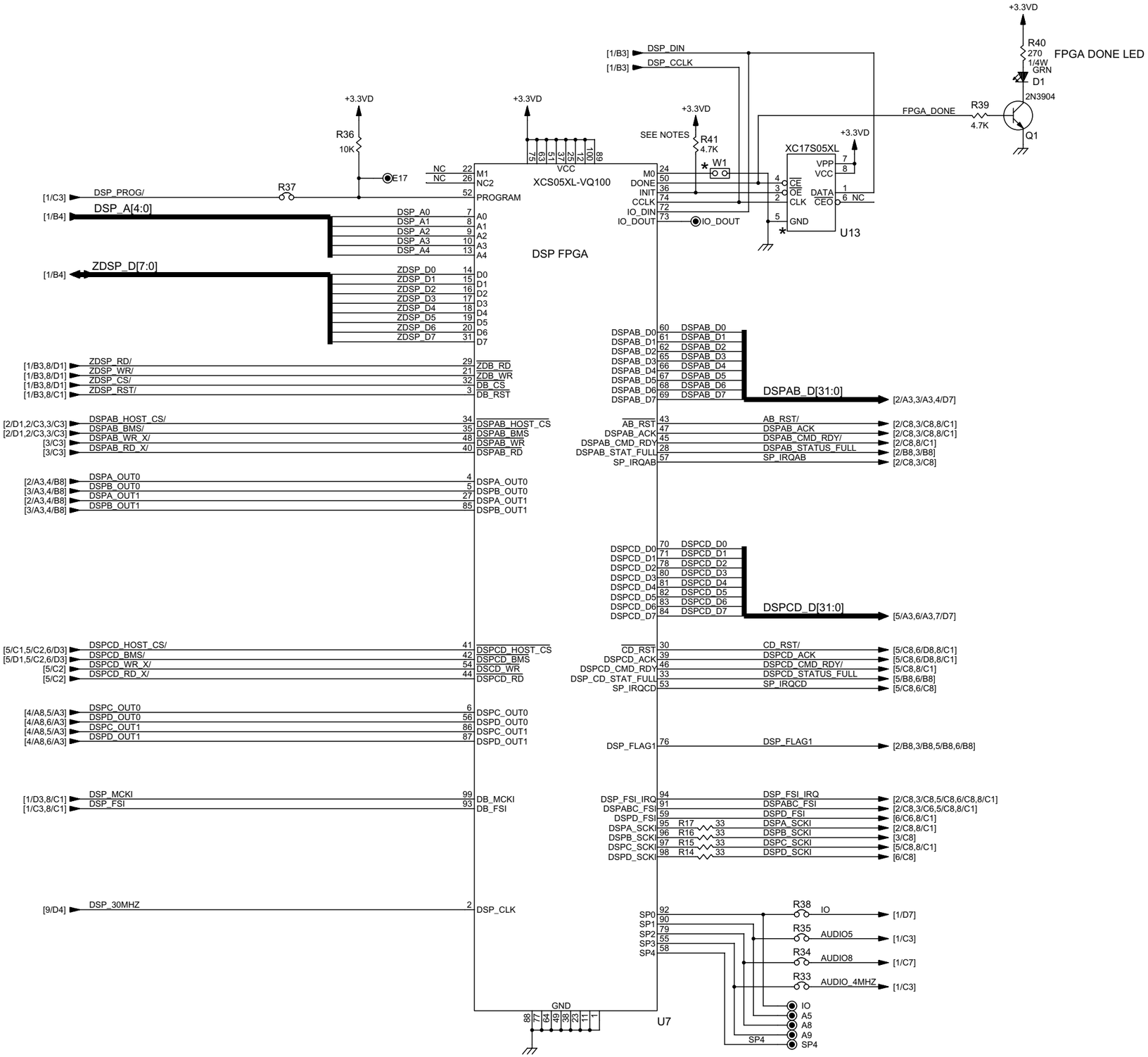
APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

TITLE
SCHEM,DSP BD,MC8
DSPCD EXT MEM

SIZE	CODE	NUMBER	REV
B		060-15309	1

FILE NAME 15309-2.7 SHEET 7 OF 9

11-18-2002_15:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02
2	CHANGE SIGNAL AUDIO9 TO AUDIO_4MHZ PER DCR 020927-00	CW 9/30/02	RWH 10/15/02
		KAB 10/15/02	KAB 10/15/02

NOTES

1 M1,M0 HAVE WEAK PULLUPS
M1,M0 = 1,1 SLAVE SERIAL MODE
M1,M0 = 1,0 MASTER SERIAL MODE

2 JUMPER W1 TO GND TO USE CONFIGURATION ROM.

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

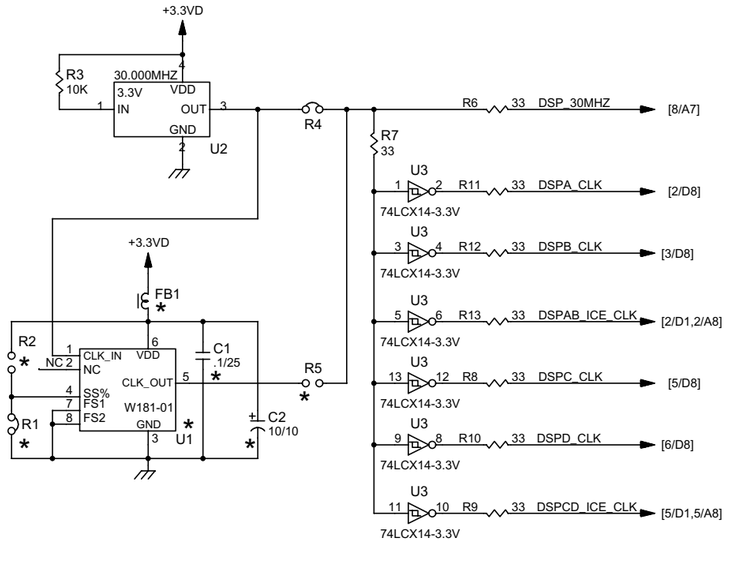
APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

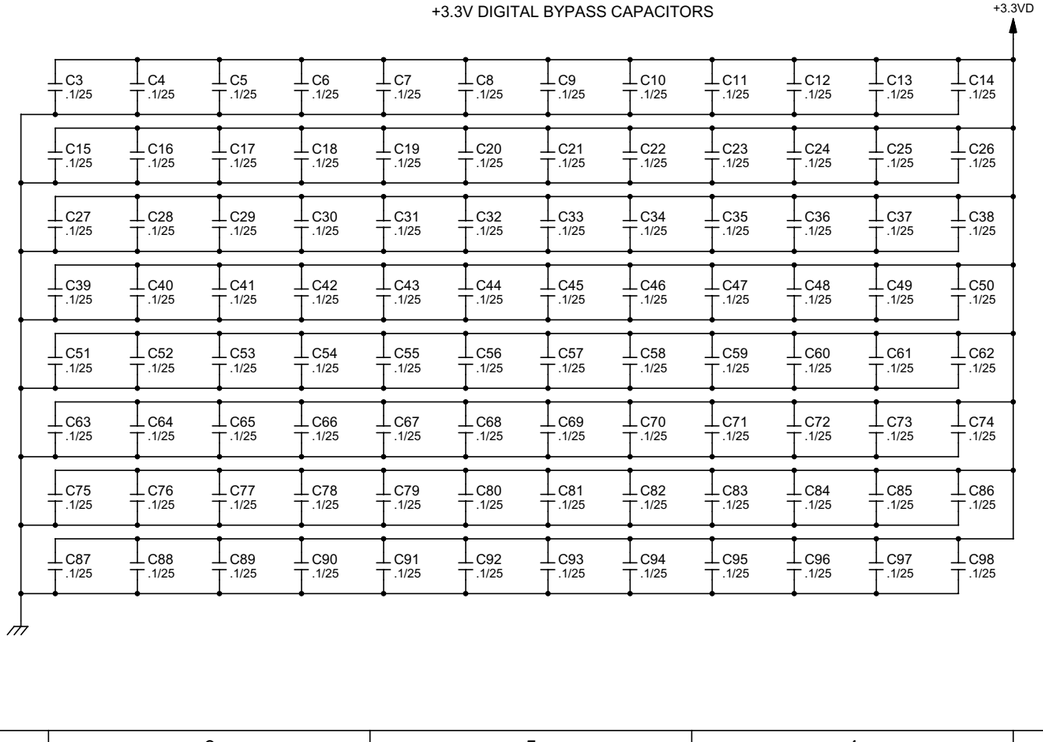
TITLE: SCHEM,DSP BD,MC8 FPGA

SIZE	CODE	NUMBER	REV
B		060-15309	2

FILE NAME: 15309-2.8 SHEET 8 OF 9

11-18-2002_15:51





REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020429-00	RWH 5/3/02	CW 5/7/02
		KAB 5/6/02	KAB 5/13/02

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

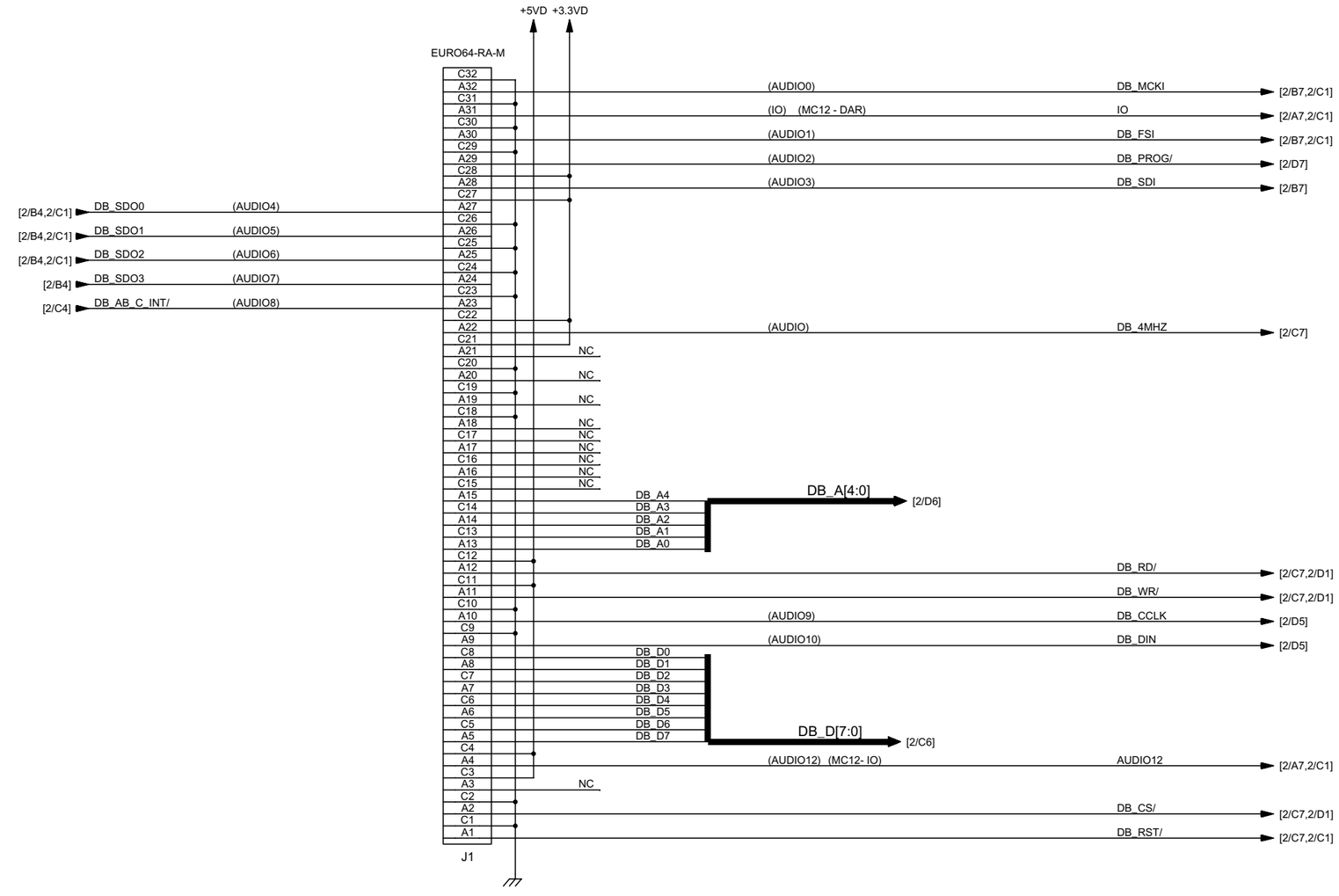
TITLE
SCHEM,DSP BD,MC8
BYPASS CAPACITORS & DSP CLOCKS

SIZE	CODE	NUMBER	REV
B		060-15309	1

FILE NAME 15309-2.9

SHEET 9 OF 9

11-18-2002 15:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020604-00	RWH 6/10/02	CW 6/24/02
		KB 6/12/02	KB 6/24/02
2	CHANGED PER DCR 020814-00	RWH 8/29/02	CW 9/5/02
		KB 9/5/02	KB 9/9/02

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C28, D3, FB1, J1, Q1, R8, RP6, U6, W1.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

8. NAMES IN PARENTHESES DESIGNATE GENERIC NOMENCLATURE USED ON THE MATING CONNECTOR OF THE MAIN BOARD SCHEMATIC.

DOCUMENT CONTROL BLOCK: #060-15319

SHEET	REV	DESCRIPTION
1 OF 4	2	MAIN BD CONNECTOR
2 OF 4	2	FPGA
3 OF 4	2	DOLBY DIGITAL/DTS DECODER
3 OF 4	2	REGULATOR & BYPASS CAPS

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

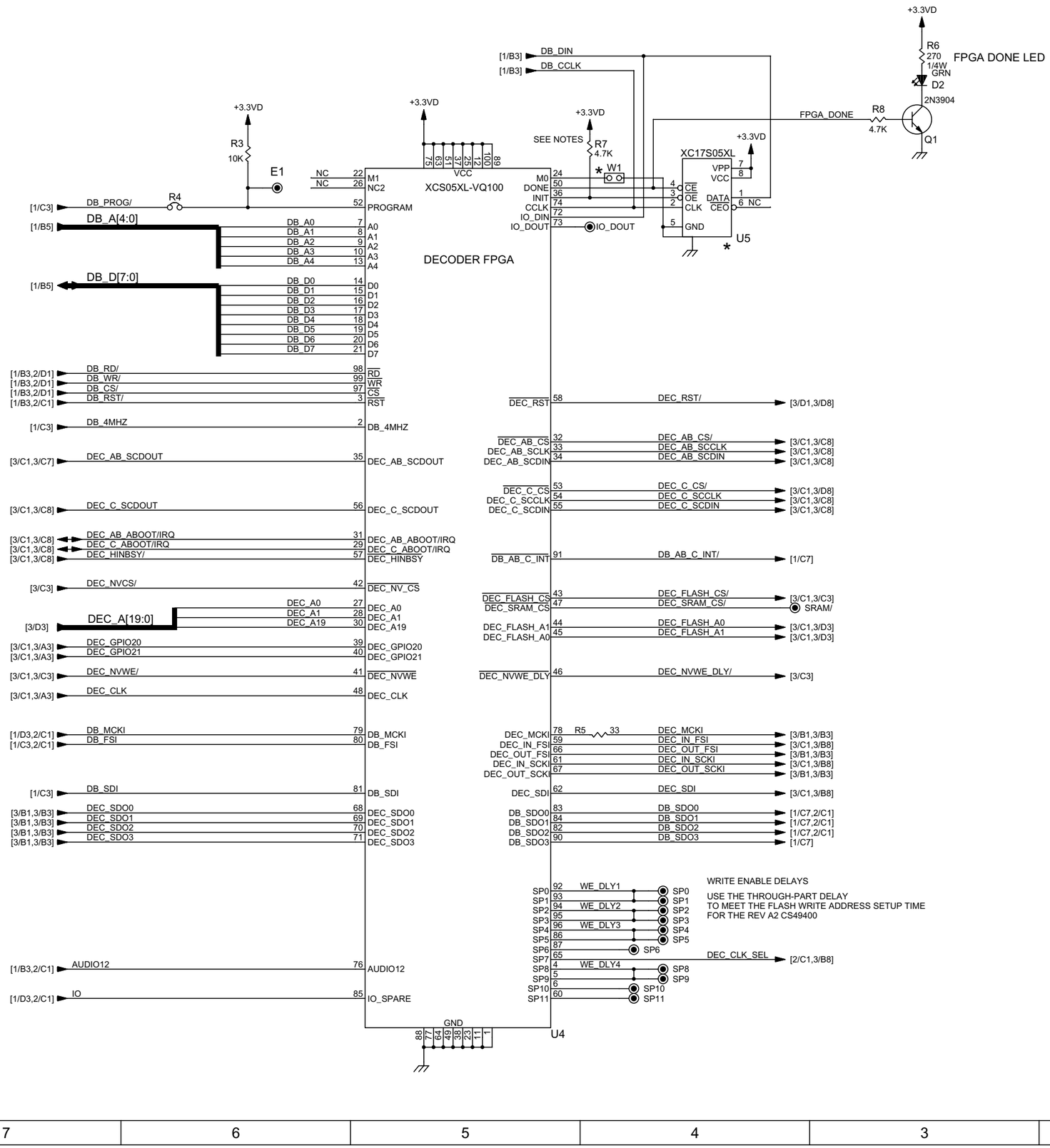
APPROVALS		DATE
DRAWN	RWH	3/21/02
CHECKED	KB	3/26/02
Q.C.	CW	3/26/02
ISSUED	KB	3/26/02

TITLE
SCHEM,DECODER BD,MC8/MC12
MAIN BD CONNECTOR

SIZE	CODE	NUMBER	REV
B		060-15319	2

FILE NAME 15319-2.1 SHEET 1 OF 4

10-23-2002_14:31



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020604-00	RWH 6/10/02	CW 6/24/02
		KB 6/12/02	KB 6/24/02
2	CHANGED PER DCR 020814-00	RWH 8/29/02	CW 9/5/02
		KB 9/5/02	KB 9/9/02

NOTES

1 M1,M0 HAVE WEAK PULLUPS
M1,M0 = 1,1 SLAVE SERIAL MODE
M1,M0 = 1,0 MASTER SERIAL MODE

2 JUMPER W1 TO GND TO USE CONFIGURATION ROM.

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	2/28/02
CHECKED	KB	3/5/02
Q.C.	CW	3/5/02
ISSUED	KB	3/5/02

TITLE: SCHEM,DECODER BD,MC8/MC12 FPGA

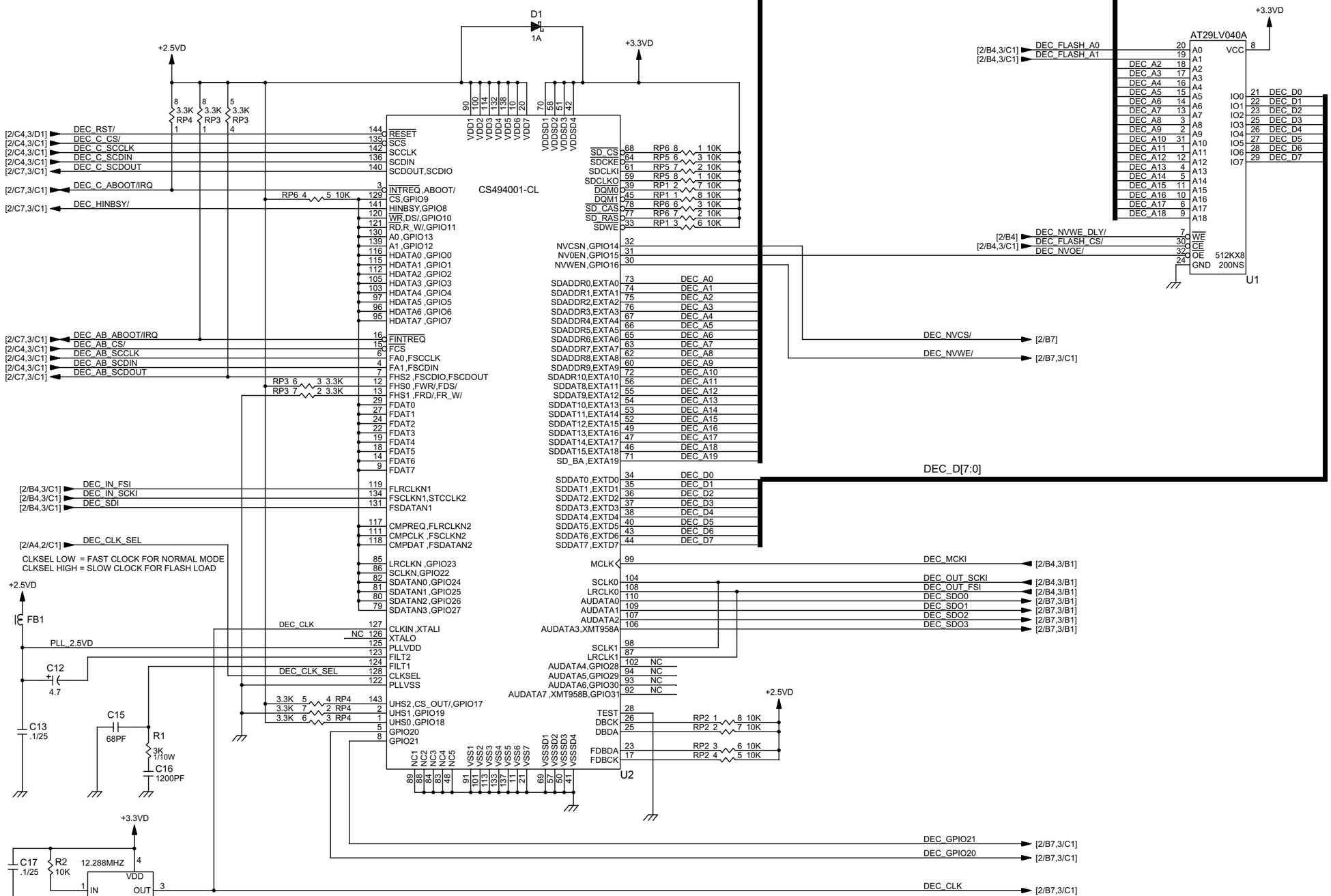
SIZE	CODE	NUMBER	REV
B		060-15319	2

FILE NAME: 15319-2.2 SHEET 2 OF 4

10-23-2002_14:48

CS49400 ABOOT/IRQ PINS ARE DUAL PURPOSE OPEN DRAIN I/O
WHEN RESET RISES WITH ABOOT LOW - > AUTOBOOT MODE
AT RUN TIME, PIN IS THE IRQ OUTPUT
PIN SHOULD NOT BE DRIVEN EXTERNALLY WHEN CHIP IS IN RUN MODE

CS49400 REQUIRES 2.5 VOLT SUPPLY
PINS ARE 3.3 VOLT TOLERANT



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020604-00	RWH 6/10/02	CW 6/24/02
		KB 6/12/02	KB 6/24/02
2	CHANGED PER DCR 020814-00	RWH 8/29/02	CW 9/5/02
		KB 9/5/02	KB 9/9/02

SPARES

NC RP1 5 4 10K NC
NC RP5 4 5 10K NC

TEST POINTS

DRST DEC_RST/
DCLK DEC_CLK
ABIRQ DEC_AB_ABOOT/IRQ
CIRQ DEC_C_ABOOT/IRQ
HINBSY DEC_HINBSY/
ABCS/ DEC_AB_CS/
ABCK DEC_AB_SCCLK
ABIN DEC_AB_SCDIN
ABOUT DEC_AB_SCDOUT
CCS/ DEC_C_CS/
CCK DEC_C_SCCLK
CIN DEC_C_SCDIN
COUT DEC_C_SCDOUT
A1 DEC_A1
A0 DEC_A0
G21 DEC_GPIO21
G20 DEC_GPIO20
FA0 DEC_FLASH_A0
FA1 DEC_FLASH_A1
NVOE/ DEC_NVOE/
NVWE/ DEC_NVWE/
FLASHCS/ DEC_FLASH_CS/
INFSI DEC_IN_FSI
INSCKI DEC_IN_SCKI
SDI DEC_SDI
MCKI DEC_MCKI
OUTFSI DEC_OUT_FSI
OUTSCKI DEC_OUT_SCKI
SDO0 DEC_SDO0
SDO1 DEC_SDO1
SDO2 DEC_SDO2
SDO3 DEC_SDO3

NOTES

1. TO SELECT SERIAL INTERFACE
   AT RISING EDGE OF RESET

   DSP AB
   FSH2 (PIN7), IS PULLED HIGH
   FHS1 (PIN13), IS PULLED LOW
   FSH0 (PIN12), IS PULLED HIGH

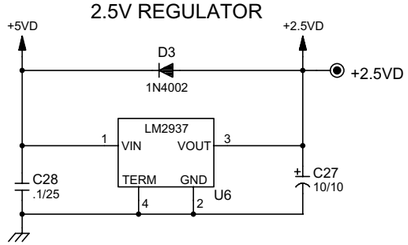
   DSP C
   USH2 (PIN143), IS PULLED HIGH
   USH1 (PIN2), IS PULLED LOW
   UHS0 (PIN1), IS PULLED HIGH

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM,DECODER BD,MC8/MC12 DOLBY DIGITAL/DTS DECODER
DRAWN	RWH	3/21/02	
CHECKED	KB	3/26/02	SIZE B / CODE / NUMBER 060-15319 / REV 2
Q.C.	CW	3/26/02	
ISSUED	KB	3/26/02	FILE NAME 15319-2.3 / SHEET 3 OF 4

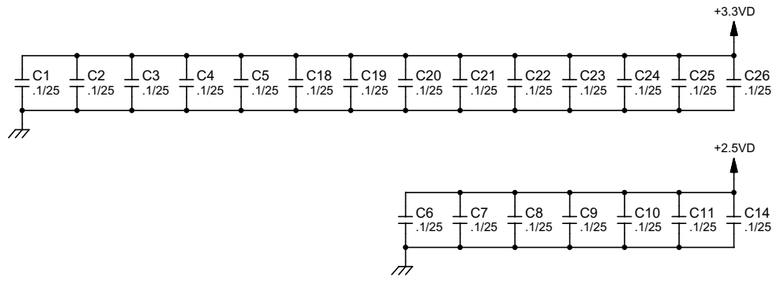
10-23-2002_14:48

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 020604-00	RWH 6/10/02	CW 6/24/02
		KB 6/12/02	KB 6/24/02
2	CHANGED PER DCR 020814-00	RWH 8/29/02	CW 9/5/02
		KB 9/5/02	KB 9/9/02

2.5V REGULATOR

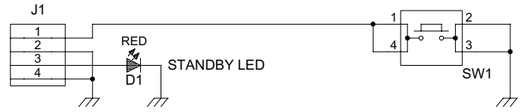


BYPASS CAPACITORS



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730
APPROVALS	DATE	TITLE: SCHEM,DECODER BD,MC8/MC12 REGULATOR & BYPASS CAPS
DRAWN RWH	3/21/02	SIZE B | CODE | NUMBER 060-15319 | REV 2
CHECKED KB	3/26/02	
Q.C. CW	3/26/02	FILE NAME 15319-2.4 | SHEET 4 OF 4
ISSUED KB	3/26/02	

10-23-2002 14:48



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 DIGITAL GROUND | ANALOG GROUND | CHASSIS GROUND | POWER GROUND

2 LAST REFERENCE DESIGNATORS USED: D1, J1, SW1

REFERENCE COPY

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	12/7/01
CHECKED	KAB	1/4/02
Q.C.	CW	1/8/02
ISSUED	KAB	1/8/02

TITLE: SCHEM,STANDBY BD, MC8

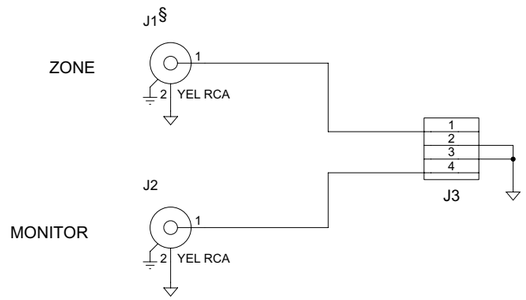
SIZE	CODE	NUMBER	REV
B		060-15329	0

FILE NAME: 15329-0.1

SHEET 1 OF 1

1-16-2002_12:48

VIDEO BOARD CONNECTOR



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	UPDATED FOR MC4 PER DCR 040922-00	RWH 9/24/04	CW 10/14/04
		AT 9/27/04	AT 9/27/04

NOTES

1 LAST REFERENCE DESIGNATORS USED: J3
2 COMPONENTS MARKED WITH § ARE NOT ON INSTALLED ON MC4.

OCT 27 2004

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

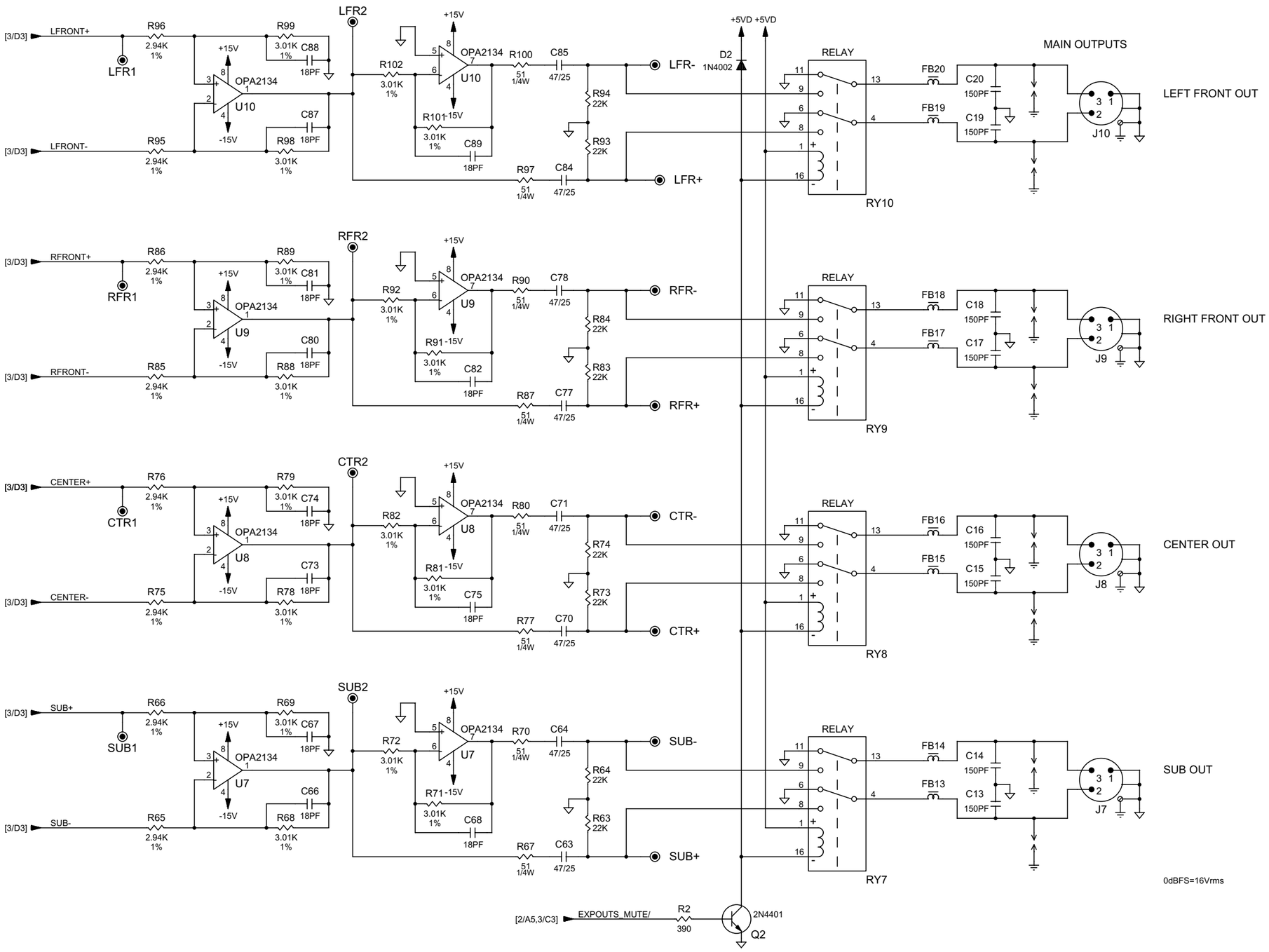
APPROVALS		DATE
DRAWN	RWH	1/9/02
CHECKED	ECM	1/10/02
Q.C.	CW	1/10/02
ISSUED	KAB	1/11/02

TITLE
SCHEM,VIDEO OUT BD,MC4/MC8
RCA OUTPUTS

SIZE	CODE	NUMBER	REV
B		060-15339	1

FILE NAME 15339-1 .1 SHEET 1 OF 1

10-19-2004_8:24



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C92, D2, FB22, J11, Q2, R102 RY10, U10.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

DOCUMENT CONTROL BLOCK: #060-15349

SHEET NUMBER	REVISION	TITLE
1 OF 3	0	FRONT,CENTER,SUB OUTPUTS
2 OF 3	0	SIDE,REAR OUTPUTS
3 OF 3	0	ZONE2 OUTPUTS

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

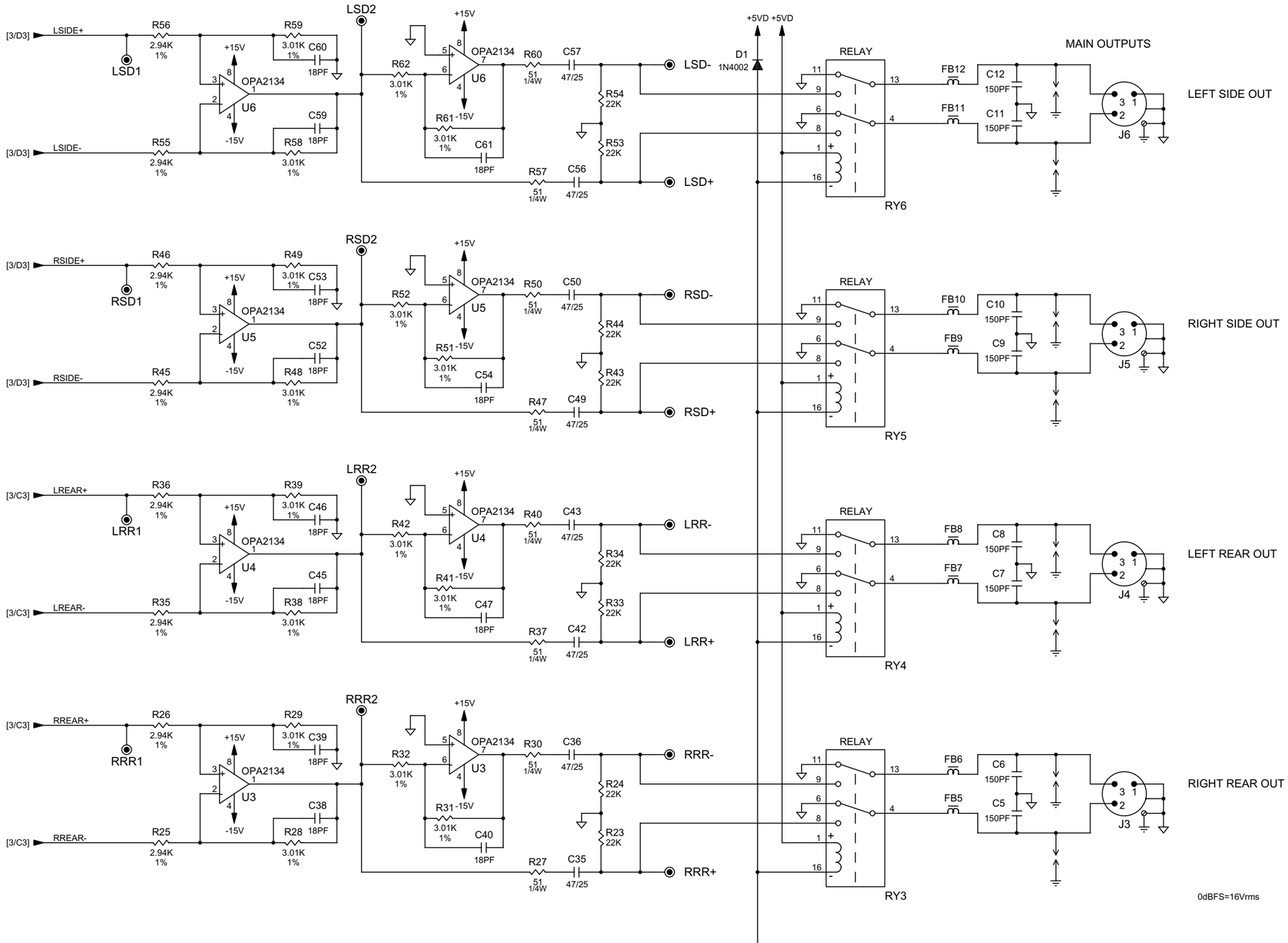
APPROVALS		DATE
DRAWN	CW	4/8/02
CHECKED	CV	4/9/02
Q.C.	RWH	4/9/02
ISSUED	KAB	4/10/02

TITLE: SCHEM,XLR BD,MC-8B FRONT,CENTER,SUB OUTPUTS

SIZE	CODE	NUMBER	REV
B		060-15349	0

FILE NAME: 15349-0.1 SHEET 1 OF 3

4-12-2002_11:43



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	CW	4/8/02
CHECKED	CV	4/9/02
Q.C.	RWH	4/9/02
ISSUED	KAB	4/10/02

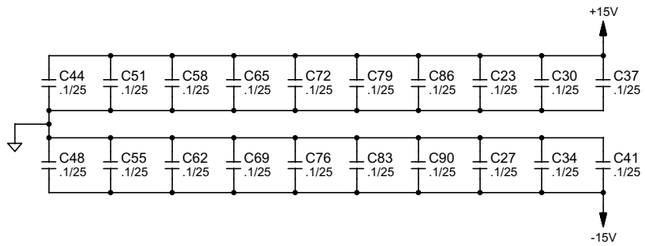
TITLE: SCHEM,XLR BD,MC-8B SIDE,REAR OUTPUTS

SIZE	CODE	NUMBER	REV
B		060-15349	0

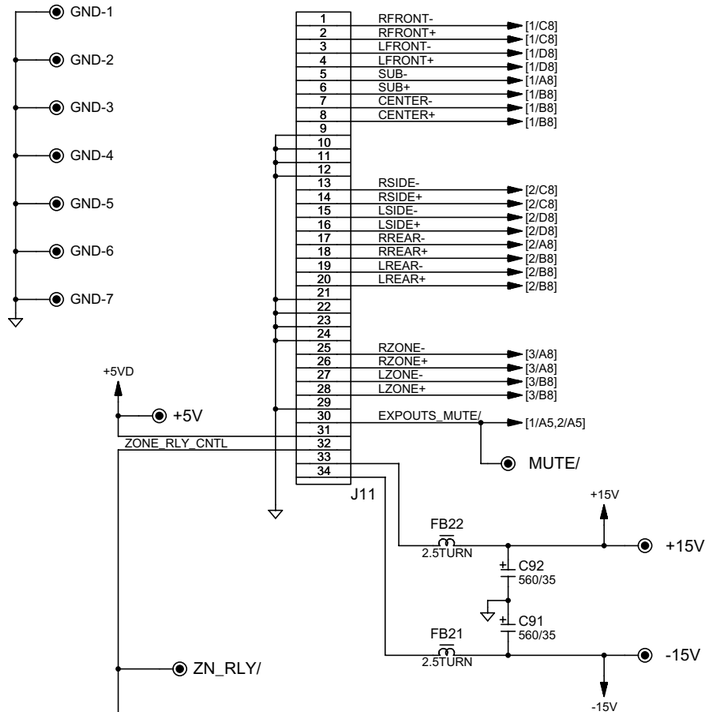
FILE NAME: 15349-0.2 SHEET 2 OF 3

4-12-2002_11:43

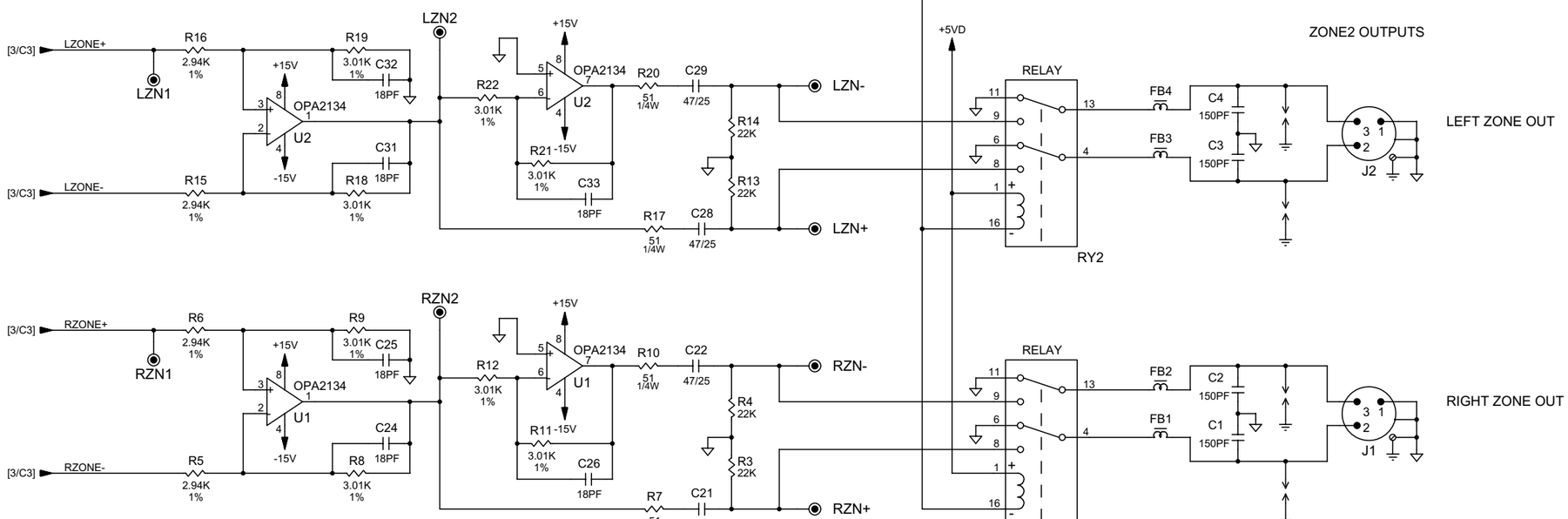
BYPASS CAPACITORS



FROM ANALOG I/O BOARD



ZONE2 OUTPUTS



0dBFS=2.0Vrms

0dBFS=4.0Vrms

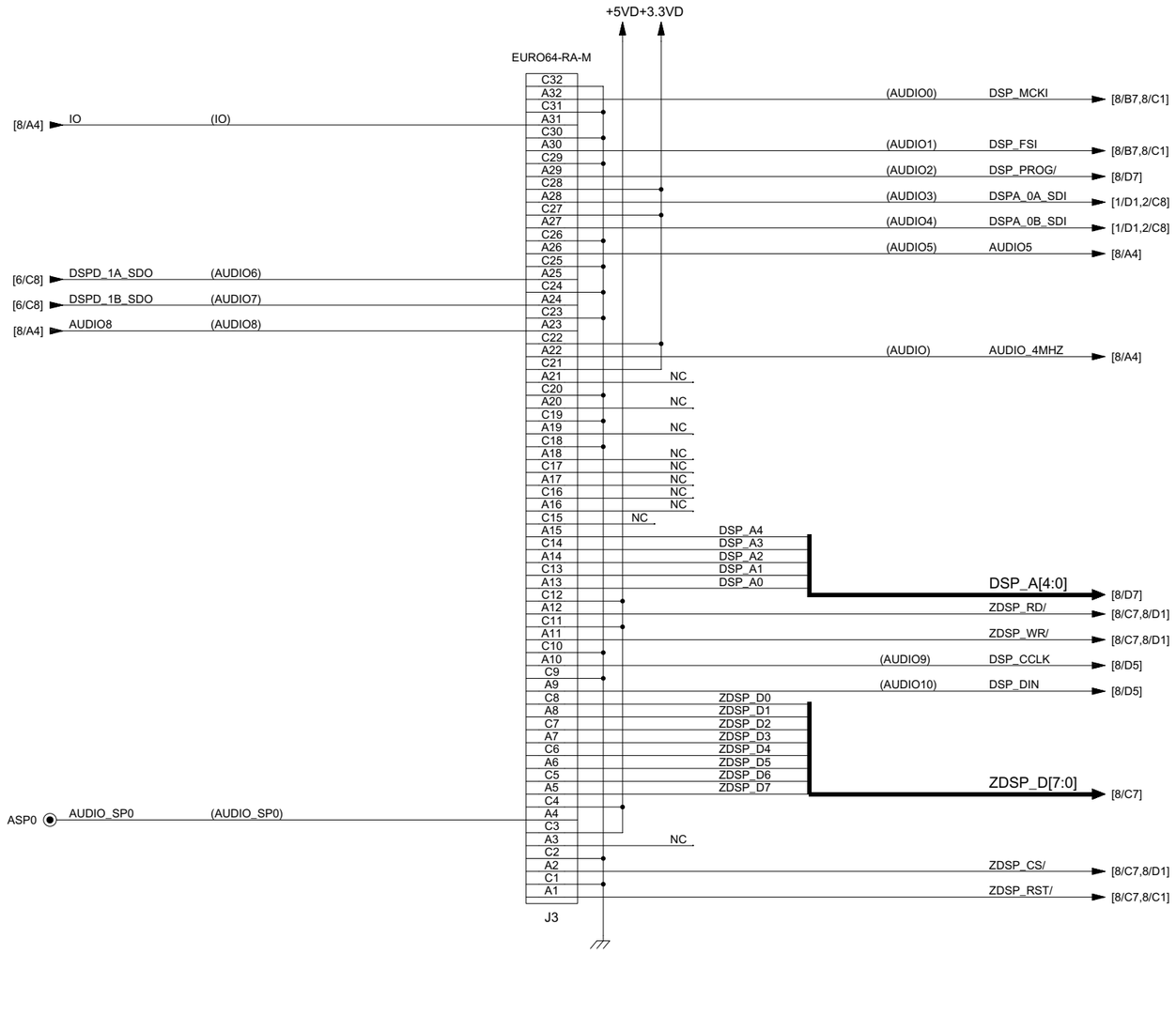
REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM,XLR BD,MC-8B ZONE2 OUTPUTS
DRAWN	CW	4/8/02	
CHECKED	CV	4/9/02	SIZE B | CODE | NUMBER 060-15349 | REV 0
Q.C.	RWH	4/9/02	
ISSUED	KAB	4/10/02	FILE NAME 15349-0.3 | SHEET 3 OF 3

4-12-2002_11:43



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REVISED SIGNAL NAMES ON SHEETS 1,8; ADD NOTE 8 PER DCR 020926-00	CW 9/27/02	RWH 10/15/02
		KAB 10/11/02	KAB 10/15/02
2	SHOW DEPOPULATION FOR MIC BD. ON SHTS. 2-8 & 10 PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

TEST POINTS

A0A_SDI — DSPA_0A_SDI
A0B_SDI — DSPA_0B_SDI

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C150, D11, FB14, J8, Q1, R95, U26, W1.

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

8 COMPONENTS MARKED WITH § ARE NOT INSTALLED ON MIC BD.

9 NAMES IN PARENTHESES DESIGNATE GENERIC NOMENCLATURE USED ON THE MATING CONNECTOR OF THE MAIN BOARD SCHEMATIC.

DOCUMENT CONTROL BLOCK: #060-15389

SHEET	REV	DESCRIPTION
1 OF 10	2	MAIN BD CONNECTOR
2 OF 10	1	DSP A
3 OF 10	1	DSP B
4 OF 10	1	DSPAB EXT MEM
5 OF 10	1	DSP C
6 OF 10	1	DSP D
7 OF 10	1	DSPCD EXT MEM
8 OF 10	2	FPGA
9 OF 10	0	MICROPHONE INPUTS
10 OF 10	1	BYPASS CAPACITORS & DSP CLOCKS

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CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	5/20/02
CHECKED	KB	5/29/02
Q.C.	CW	6/3/02
ISSUED	KB	6/3/02

TITLE
SCHEM,MIC/DSP BD,MC8
MAIN BD CONNECTOR

SIZE	CODE	NUMBER	REV
B		060-15389	2

FILE NAME 15389-2.1 SHEET 1 OF 10

12-28-2004_16:35

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

MASTER - ID0 HIGH, ID1 LOW
SLAVE - ID0 LOW, ID1 HIGH

+3.3VD

R66 § R67 §

VCC

ADSP21065

[10/D6]	DSPA_CLK	DSPA_CLK	30	CLKIN	
		NC	31	XTAL2	
[3/C8,8/C4,8/C1]	AB_RST/		152	BSEL	
			157	RESET	
			144	ID0	
			143	ID1	
[3/C8,8/C4,8/C1]	DSPAB_ACK	DSPAB_ACK	69	ACK	
[3/C8,5/C8,6/C8,8/B4,8/C1]	DSP_FSI_IRQ		205	IRQ0	
[3/C8,8/C4]	SP_IRQAB		206	IRQ1	
[8/C4,8/C1]	DSPAB_CMD_RDY/		207	IRQ2	
[3/C6,5/C8,8/B4,8/C1]	DSPABC_FSI		2	RFS0	
[8/B4,8/C1]	DSPA_SCKI		4	RCLK0	
[1/D1,1/C3]	DSPA_0A_SDI		5	DR0A	
[1/D1,1/C3]	DSPA_0B_SDI		6	DR0B	
			7	TFS0	
		NC	8	TCLK0	
		NC	11	DT0A	
		NC	12	DT0B	
			13	RFS1	
		NC	15	RCLK1	
			16	DR1A	
			17	DR1B	
			18	TFS1	
		NC	19	TCLK1	
		NC	22	DT1A	
		NC	23	DT1B	
		NC	26	PWMEVENT0	
		NC	24	PWMEVENT1	
			38	DMAR1	
			39	DMAR2	
			50	DMAG1	
			51	DMAG2	
			40	HBR	
		NC	52	HBG	
			55	CS	
		NC	63	REDY	
			56	SBTS	
[2/C1,3/B8]	DSPAB_CPA/	R65 §	65	CPA	
[2/C1,3/B8]	DSPAB_BR1/		27	BR1	
[2/C1,3/B8]	DSPAB_BR2/		28	BR2	
		DSPAB_EMU/	145	EMU	
		DSPA_TDO	146	TDO	
		DSPAB_TDI	148	TDI	
		DSPAB_TCK	151	TCK	
		DSPAB_TMS	149	TMS	
		DSPAB_TRST	147	TRST	
[3/B8,8/C4]	DSPAB_STATUS_FULL		197	FLAG0	
[3/B8,5/B8,6/B8,8/B4]	DSP_FLAG1		198	FLAG1	
		NC	199	FLAG2	
			201	FLAG3	AF3
			138	FLAG4	AF4
			137	FLAG5	AF5
			136	FLAG6	AF6
			134	FLAG7	AF7
			80	FLAG8	AF8
			79	FLAG9	
			78	FLAG10	
		NC	76	FLAG11	
		NC	102	NC1	
		NC	103	NC2	
		NC	115	NC3	
		NC	142	NC4	
		NC	202	NC5	
		NC	203	NC6	

RAS	42	DSPAB_RAS/		[2/D1,3/D3,4/C8]
CAS	43	DSPAB_CAS/		[2/D1,3/D3,4/C8]
SDWE	44	DSPAB_SDWE/		[2/D1,3/D3,4/C8]
DQM	46	DSPAB_DQM		[2/D1,3/D3,4/C8]
SDCKE	47	DSPAB_SDCKE		[2/D1,3/D3,4/C8]
SDA10	48	DSPAB_SDA10		[2/D1,3/D3,4/D8]
SDCLK0	37	DSPAB_SDCLK		[2/D1,3/D3,4/C8]
SDCLK1	34	NC		
BMS	153	DSPAB_BMS/		
MS0	70	DSPAB_SDRAM_CS/		[2/D1,3/C3,8/C7]
MS1	71	DSPAB_HOST_CS/		[2/D1,3/C3,4/C8]
MS2	74	DSPAB_SRAM_CS/		[2/D1,3/C3,8/C7]
MS3	75	NC		[2/D1,3/C3,4/D4]
SW	64	NC		
WR	58	DSPAB_WR/		[2/D1,3/C3,4/B4]
RD	59	DSPAB_RD/		[2/D1,3/C3,4/B4]
A0	195	DSPAB_A0		
A1	194	DSPAB_A1		
A2	193	DSPAB_A2		
A3	190	DSPAB_A3		
A4	189	DSPAB_A4		
A5	188	DSPAB_A5		
A6	185	DSPAB_A6		
A7	184	DSPAB_A7		
A8	183	DSPAB_A8		
A9	180	DSPAB_A9		
A10	179	DSPAB_A10		
A11	178	DSPAB_A11		
A12	175	DSPAB_A12		
A13	174	DSPAB_A13		
A14	173	DSPAB_A14		
A15	171	DSPAB_A15		
A16	170	DSPAB_A16		
A17	169	DSPAB_A17		
A18	166	DSPAB_A18		
A19	165	DSPAB_A19		
A20	164	DSPAB_A20		
A21	162	DSPAB_A21		
A22	161	DSPAB_A22		
A23	160	DSPAB_A23	DSPAB_A[23:0]	[3/B3,4/D6]
D0	82	DSPAB_D0		
D1	83	DSPAB_D1		
D2	84	DSPAB_D2		
D3	86	DSPAB_D3		
D4	87	DSPAB_D4		
D5	88	DSPAB_D5		
D6	90	DSPAB_D6		
D7	91	DSPAB_D7		
D8	92	DSPAB_D8		
D9	96	DSPAB_D9		
D10	97	DSPAB_D10		
D11	98	DSPAB_D11		
D12	100	DSPAB_D12		
D13	101	DSPAB_D13		
D14	104	DSPAB_D14		
D15	107	DSPAB_D15		
D16	108	DSPAB_D16		
D17	109	DSPAB_D17		
D18	111	DSPAB_D18		
D19	112	DSPAB_D19		
D20	113	DSPAB_D20		
D21	116	DSPAB_D21		
D22	117	DSPAB_D22		
D23	118	DSPAB_D23		
D24	121	DSPAB_D24		
D25	122	DSPAB_D25		
D26	123	DSPAB_D26		
D27	126	DSPAB_D27		
D28	127	DSPAB_D28		
D29	128	DSPAB_D29		
D30	132	DSPAB_D30		
D31	133	DSPAB_D31	DSPAB_D[31:0]	[3/A3,4/D7,8/C4]
BMSTR	53	DSPA_BMSTR	DSPA_BMSTR	
NC7	208	NC		

GND

U16 §

DEVELOPMENT ONLY:
PIN 7, BTCK, JUMP TO PIN 8
PIN 9, BTRST/, JUMP TO PIN 10

+3.3VD +3.3VD

R61 § R62 §

* J2

	1	2	DSPAB_EMU/	DSPA_TDO / DSPAB_EMU/ [3/B8]
NC	3	4	DSPAB_ICE_CLK	
NC	5	6	DSPAB_TMS	DSPAB_TMS [3/B8]
	7	8	DSPAB_TCK	DSPAB_TCK [3/B8]
	9	10	DSPAB_TRST	DSPAB_TRST [3/B8]
NC	11	12	DSPAB_TDI	
	13	14		

[3/B8] DSPB_TDO
[2/D1,10/C6] DSPAB_ICE_CLK

DSPA_OUT1 [4/B8,8/C7]
DSPA_OUT0 [4/B8,8/C7]

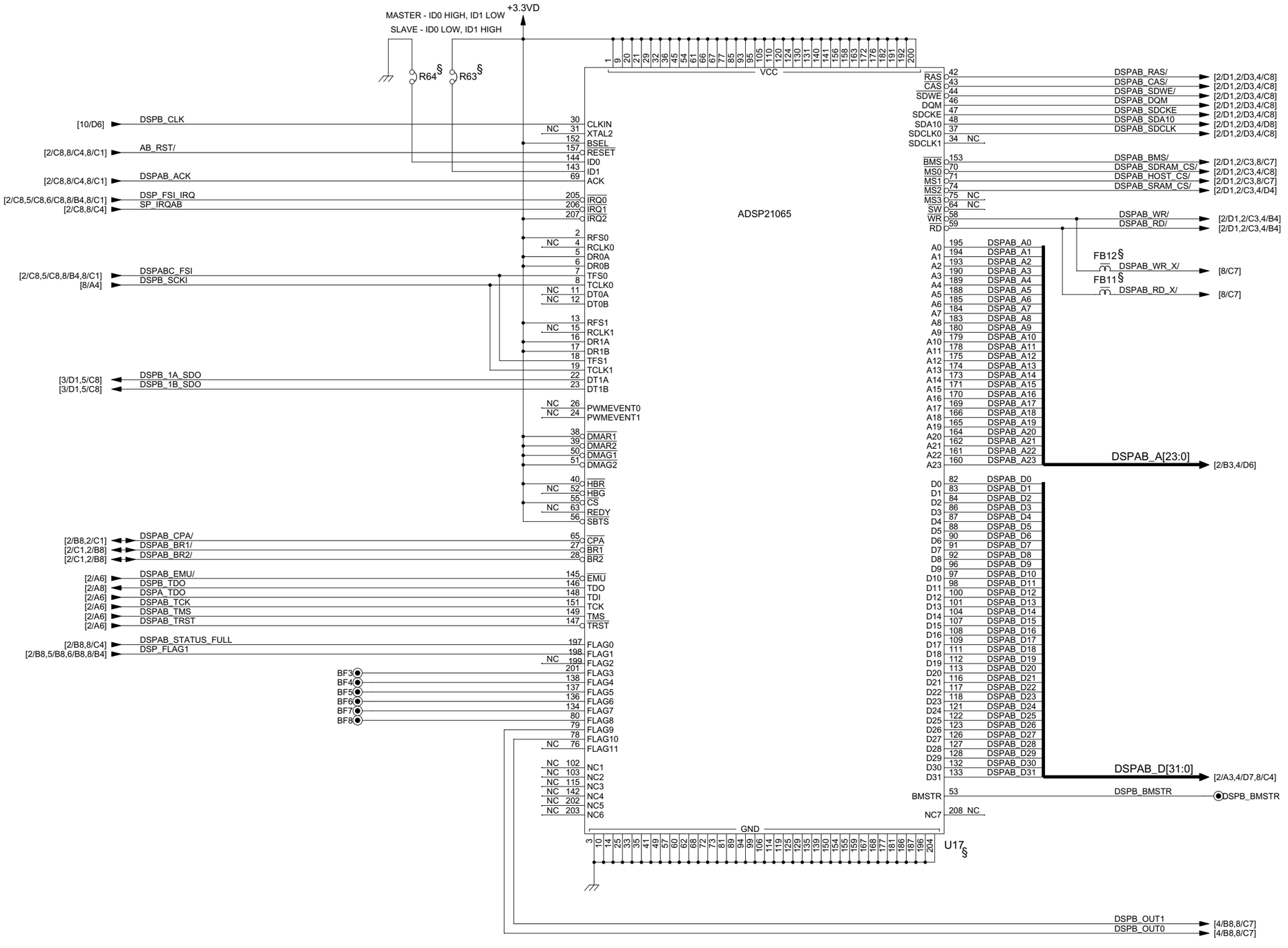
TEST POINTS

ABCLK	DSPAB_ICE_CLK
ABWR/	DSPAB_WR/
ABRD/	DSPAB_RD/
ABBMS/	DSPAB_BMS/
ABHOST_CS/	DSPAB_HOST_CS/
ABSRAM_CS/	DSPAB_SRAM_CS/
ABSDRAM_CS/	DSPAB_SDRAM_CS/
ABRAS/	DSPAB_RAS/
ABCAS/	DSPAB_CAS/
ABSDWE/	DSPAB_SDWE/
ABDQM	DSPAB_DQM
ABSDCKE	DSPAB_SDCKE
ABSDA10	DSPAB_SDA10
ABSDCLK	DSPAB_SDCLK
ABCPA/	DSPAB_CPA/
ABBR1/	DSPAB_BR1/
ABBR2/	DSPAB_BR2/

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	SCHEM,MIC/DSP BD,MC8 DSP A
DRAWN RWH	5/20/02	SIZE B	CODE / NUMBER 060-15389 / REV 1
CHECKED KB	5/29/02		
Q.C. CW	6/3/02	FILE NAME	15389-2.2
ISSUED KB	6/3/02	SHEET	2 OF 10

12-15-2004_8:52

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

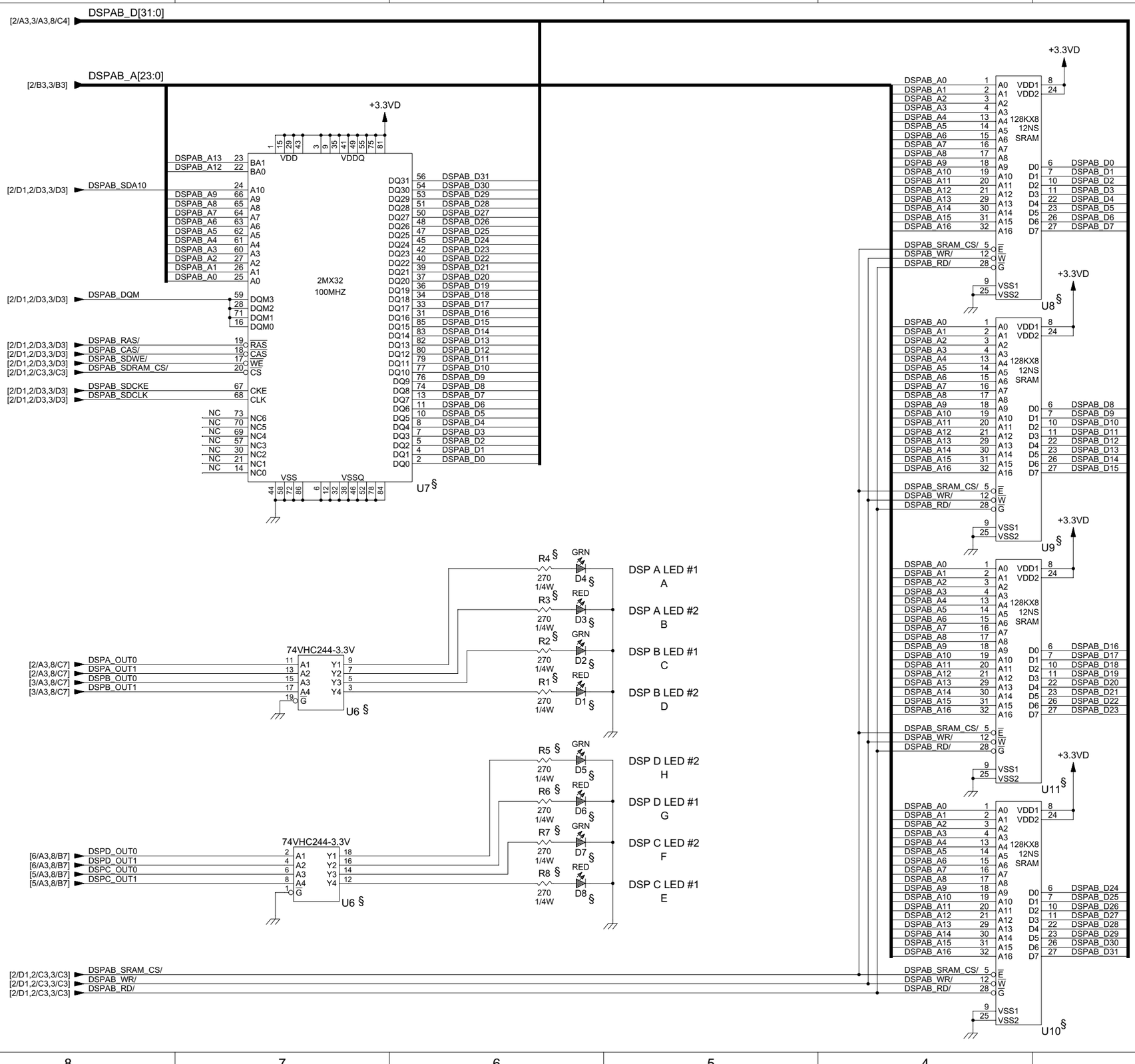


TEST POINTS

B1A_SDO DSPB_1A_SDO
B1B_SDO DSPB_1B_SDO

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MIC/DSP BD,MC8 DSP B
DRAWN	RWH	5/20/02	
CHECKED	KB	5/29/02	SIZE: B; CODE: ; NUMBER: 060-15389; REV: 1
Q.C.	CW	6/3/02	
ISSUED	KB	6/3/02	FILE NAME: 15389-2.3; SHEET 3 OF 10

12-15-2004_8:57



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	5/20/02
CHECKED	KB	5/29/02
Q.C.	CW	6/3/02
ISSUED	KB	6/3/02

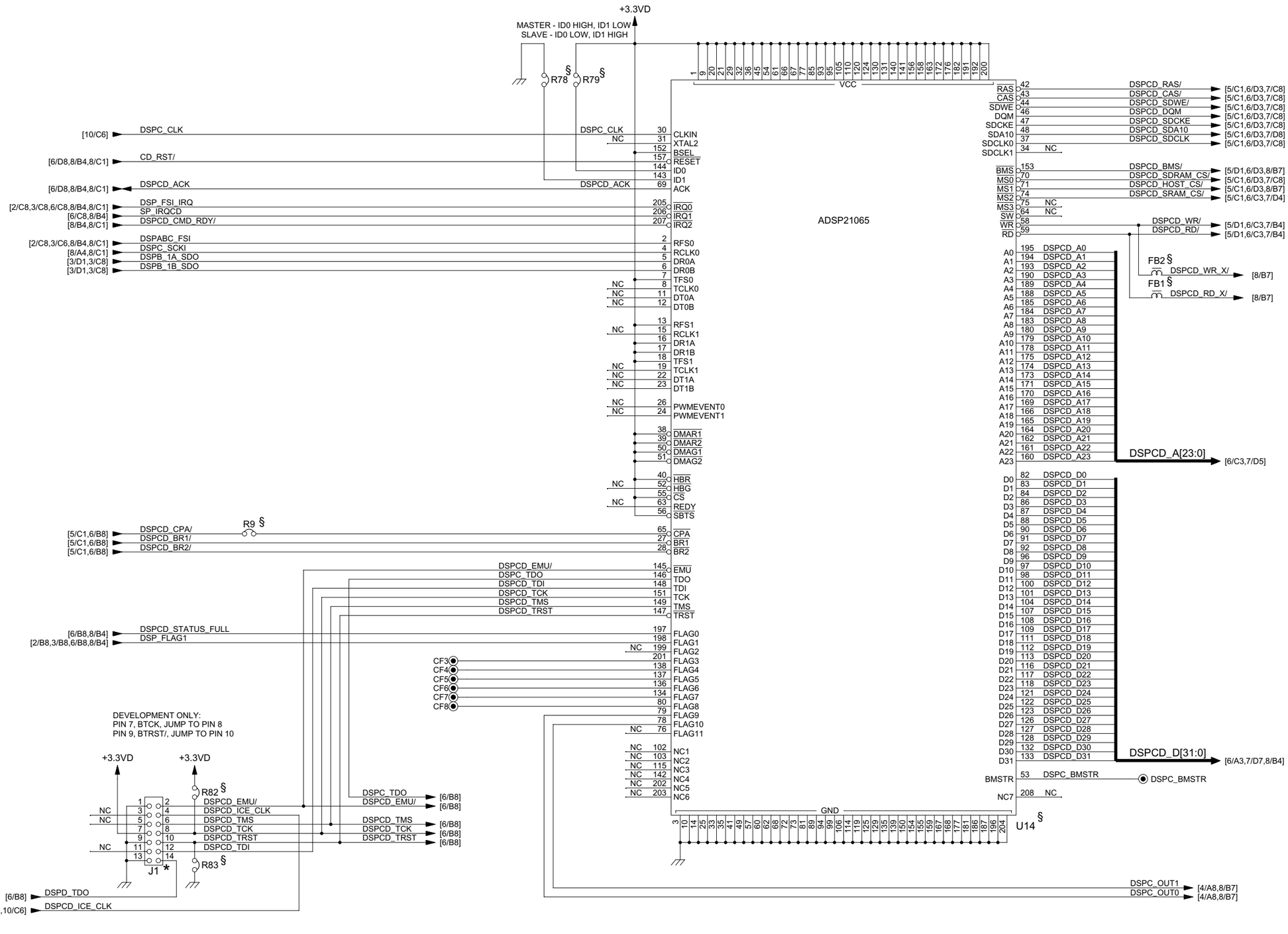
TITLE: SCHEM,MIC/DSP BD,MC8
DSPAB EXT MEM

SIZE	CODE	NUMBER	REV
B		060-15389	1

FILE NAME: 15389-2.4 SHEET 4 OF 10

12-15-2004_8:52

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04



TEST POINTS

CDCLK	DSPCD_ICE_CLK
CDWR/	DSPCD_WR/
CDRD/	DSPCD_RD/
CDBMS/	DSPCD_BMS/
CDHOST_CS/	DSPCD_HOST_CS/
CDSRAM_CS/	DSPCD_SRAM_CS/
CDSDRAM_CS/	DSPCD_SDRAM_CS/
CDRAS/	DSPCD_RAS/
CDCAS/	DSPCD_CAS/
CDSDWE/	DSPCD_SDWE/
CDDQM	DSPCD_DQM
CDDCKE	DSPCD_SDCKE
CDSDA10	DSPCD_SDA10
CDSDCLK	DSPCD_SDCLK
CDCPA/	DSPCD_CPA/
CDBR1/	DSPCD_BR1/
CDBR2/	DSPCD_BR2/

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730
APPROVALS	DATE	TITLE: SCHEM,MIC/DSP BD,MC8 DSP C
DRAWN RWH	5/20/02	
CHECKED KB	5/29/02	SIZE B / CODE / NUMBER 060-15389 / REV 1
Q.C. CW	6/3/02	
ISSUED KB	6/3/02	FILE NAME 15389-2.5 / SHEET 5 OF 10

12-15-2004 8:52

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

+3.3VD

MASTER - ID0 HIGH, ID1 LOW

SLAVE - ID0 LOW, ID1 HIGH

R81 § R80 §

VCC: 1, 9, 20, 21, 29, 32, 36, 45, 54, 61, 66, 67, 77, 85, 93, 95, 105, 110, 120, 124, 130, 131, 140, 141, 156, 158, 163, 172, 176, 182, 191, 192, 200

ADSP21065

[10/C6]	DSPD_CLK	30	CLKIN	
		NC 31	XTAL2	
		152	BSEL	
[5/C8,8/B4,8/C1]	CD_RST/	157	RESET	
		144	ID0	
		143	ID1	
[5/C8,8/B4,8/C1]	DSPCD_ACK	69	ACK	
[2/C8,3/C8,5/C8,8/B4,8/C1]	DSP_FSI_IRQ	205	IRQ0	
[5/C8,8/B4]	SP_IRQCD	206	IRQ1	
		207	IRQ2	
		2	RFS0	
		NC 4	RCLK0	
		5	DR0A	
		6	DR0B	
[8/B4,8/C1]	DSPD_FSI	7	TFS0	
[8/A4]	DSPD_SCKI	8	TCLK0	
		NC 11	DT0A	
		NC 12	DT0B	
		13	RFS1	
		NC 15	RCLK1	
		16	DR1A	
		17	DR1B	
		18	TFS1	
		19	TCLK1	
[1/C7]	DSPD_1A_SDO	22	DT1A	
[1/C7]	DSPD_1B_SDO	23	DT1B	
		NC 26	PWMEVENT0	
		NC 24	PWMEVENT1	
		38	DMAR1	
		39	DMAR2	
		50	DMAG1	
		51	DMAG2	
		40	HBR	
		NC 52	HBG	
		55	CS	
		NC 63	REDY	
		56	SBTS	
[5/B8,5/C1]	DSPCD_CPA/	65	CPA	
[5/C1,5/B8]	DSPCD_BR1/	27	BR1	
[5/C1,5/B8]	DSPCD_BR2/	28	BR2	
[5/A6]	DSPCD_EMU/	145	EMU	
[5/A8]	DSPD_TDO	146	TDO	
[5/A6]	DSPC_TDO	148	TDI	
[5/A6]	DSPCD_TCK	151	TCK	
[5/A6]	DSPCD_TMS	149	TMS	
[5/A6]	DSPCD_TRST	147	TRST	
[5/B8,8/B4]	DSPCD_STATUS_FULL	197	FLAG0	
[2/B8,3/B8,5/B8,8/B4]	DSP_FLAG1	198	FLAG1	
		NC 199	FLAG2	
DF3		201	FLAG3	
DF4		138	FLAG4	
DF5		137	FLAG5	
DF6		136	FLAG6	
DF7		134	FLAG7	
DF8		80	FLAG8	
		79	FLAG9	
		78	FLAG10	
		NC 76	FLAG11	
		NC 102	NC1	
		NC 103	NC2	
		NC 115	NC3	
		NC 142	NC4	
		NC 202	NC5	
		NC 203	NC6	

RAS	42	DSPCD_RAS/	[5/C1,5/D3,7/C8]
CAS	43	DSPCD_CAS/	[5/C1,5/D3,7/C8]
SDWE	44	DSPCD_SDWE/	[5/C1,5/D3,7/C8]
DQM	46	DSPCD_DQM	[5/C1,5/D3,7/C8]
SDCKE	47	DSPCD_SDCKE	[5/C1,5/D3,7/C8]
SDA10	48	DSPCD_SDA10	[5/C1,5/D3,7/D8]
SDCLK0	37	DSPCD_SDCLK	[5/C1,5/D3,7/C8]
SDCLK1	34 NC		
BMS	153	DSPCD_BMS/	
MS0	70	DSPCD_SDRAM_CS/	[5/D1,5/C3,8/B7]
MS1	71	DSPCD_HOST_CS/	[5/C1,5/C3,7/C8]
MS2	74	DSPCD_SRAM_CS/	[5/C1,5/C3,8/B7]
MS3	75 NC		[5/C1,5/C3,7/D4]
SW	64 NC		
WR	58	DSPCD_WR/	
RD	59	DSPD_RD/	[5/C3,5/D1,7/B4]
			[5/C3,5/D1,7/B4]

A0	195	DSPCD_A0	
A1	194	DSPCD_A1	
A2	193	DSPCD_A2	
A3	190	DSPCD_A3	
A4	189	DSPCD_A4	
A5	188	DSPCD_A5	
A6	185	DSPCD_A6	
A7	184	DSPCD_A7	
A8	183	DSPCD_A8	
A9	180	DSPCD_A9	
A10	179	DSPCD_A10	
A11	178	DSPCD_A11	
A12	175	DSPCD_A12	
A13	174	DSPCD_A13	
A14	173	DSPCD_A14	
A15	171	DSPCD_A15	
A16	170	DSPCD_A16	
A17	169	DSPCD_A17	
A18	166	DSPCD_A18	
A19	165	DSPCD_A19	
A20	164	DSPCD_A20	
A21	162	DSPCD_A21	
A22	161	DSPCD_A22	
A23	160	DSPCD_A23	DSPCD_A[23:0] [5/B3,7/D5]

D0	82	DSPCD_D0	
D1	83	DSPCD_D1	
D2	84	DSPCD_D2	
D3	86	DSPCD_D3	
D4	87	DSPCD_D4	
D5	88	DSPCD_D5	
D6	90	DSPCD_D6	
D7	91	DSPCD_D7	
D8	92	DSPCD_D8	
D9	96	DSPCD_D9	
D10	97	DSPCD_D10	
D11	98	DSPCD_D11	
D12	100	DSPCD_D12	
D13	101	DSPCD_D13	
D14	104	DSPCD_D14	
D15	107	DSPCD_D15	
D16	108	DSPCD_D16	
D17	109	DSPCD_D17	
D18	111	DSPCD_D18	
D19	112	DSPCD_D19	
D20	113	DSPCD_D20	
D21	116	DSPCD_D21	
D22	117	DSPCD_D22	
D23	118	DSPCD_D23	
D24	121	DSPCD_D24	
D25	122	DSPCD_D25	
D26	123	DSPCD_D26	
D27	126	DSPCD_D27	
D28	127	DSPCD_D28	
D29	128	DSPCD_D29	
D30	132	DSPCD_D30	
D31	133	DSPCD_D31	DSPCD_D[31:0] [5/A3,7/D7,8/B4]

BMSTR	53	DSPD_BMSTR	DSPD_BMSTR
NC7	208 NC		

GND: 3, 10, 14, 25, 33, 35, 41, 49, 57, 60, 62, 68, 72, 73, 81, 89, 94, 99, 106, 114, 119, 125, 129, 135, 139, 150, 154, 155, 159, 167, 168, 177, 181, 186, 187, 196, 204

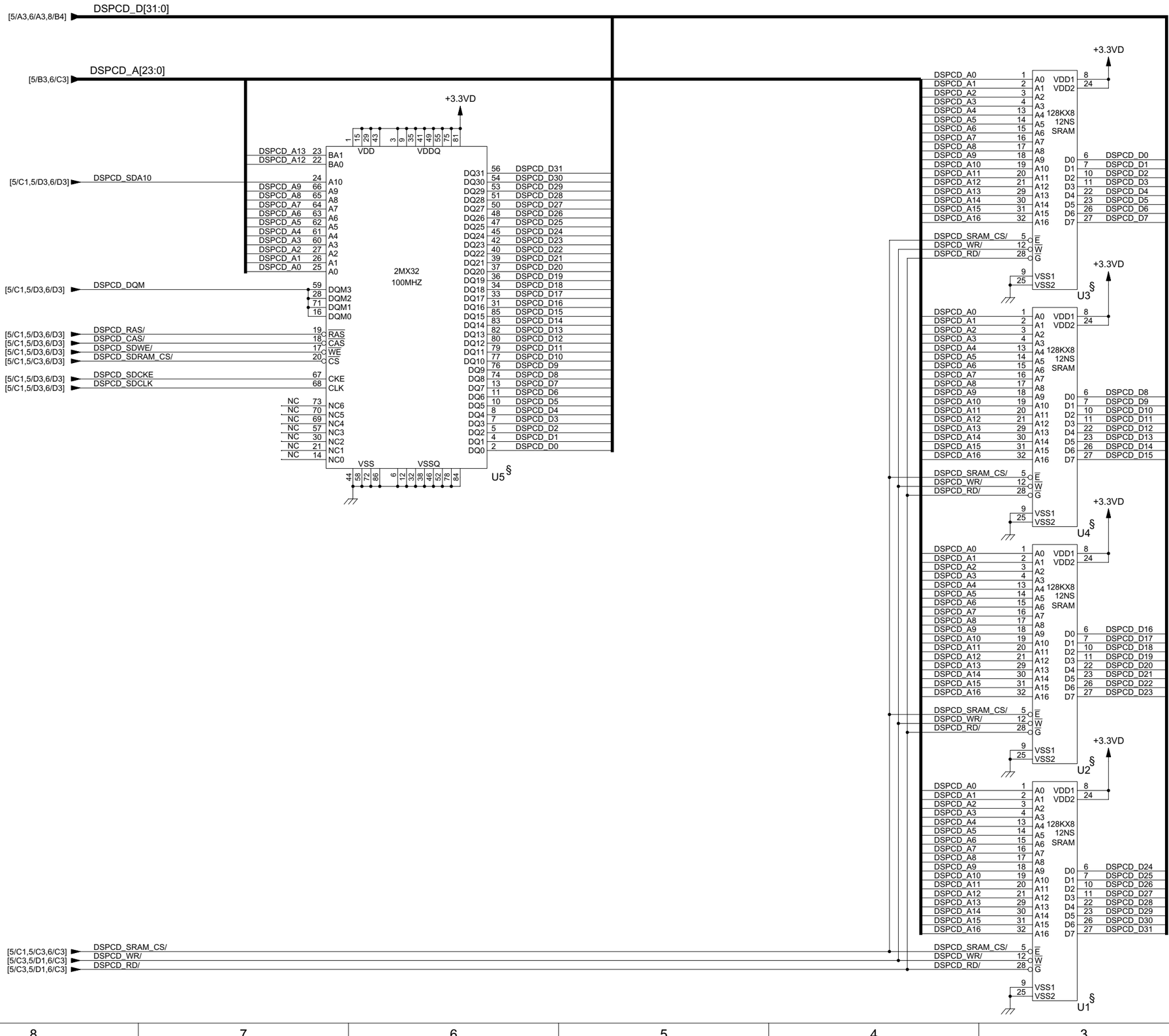
U13 §

DSPD_OUT1 → [4/A8,8/B7]

DSPD_OUT0 → [4/A8,8/B7]

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE: SCHEM,MIC/DSP BD,MC8 DSP D
DRAWN	RWH	5/20/02	
CHECKED	KB	5/29/02	SIZE B | CODE | NUMBER 060-15389 | REV 1
Q.C.	CW	6/3/02	
ISSUED	KB	6/3/02	FILE NAME 15389-2.6 | SHEET 6 OF 10

12-15-2004_8:52



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	5/20/02
CHECKED	KB	5/29/02
Q.C.	CW	6/3/02
ISSUED	KB	6/3/02

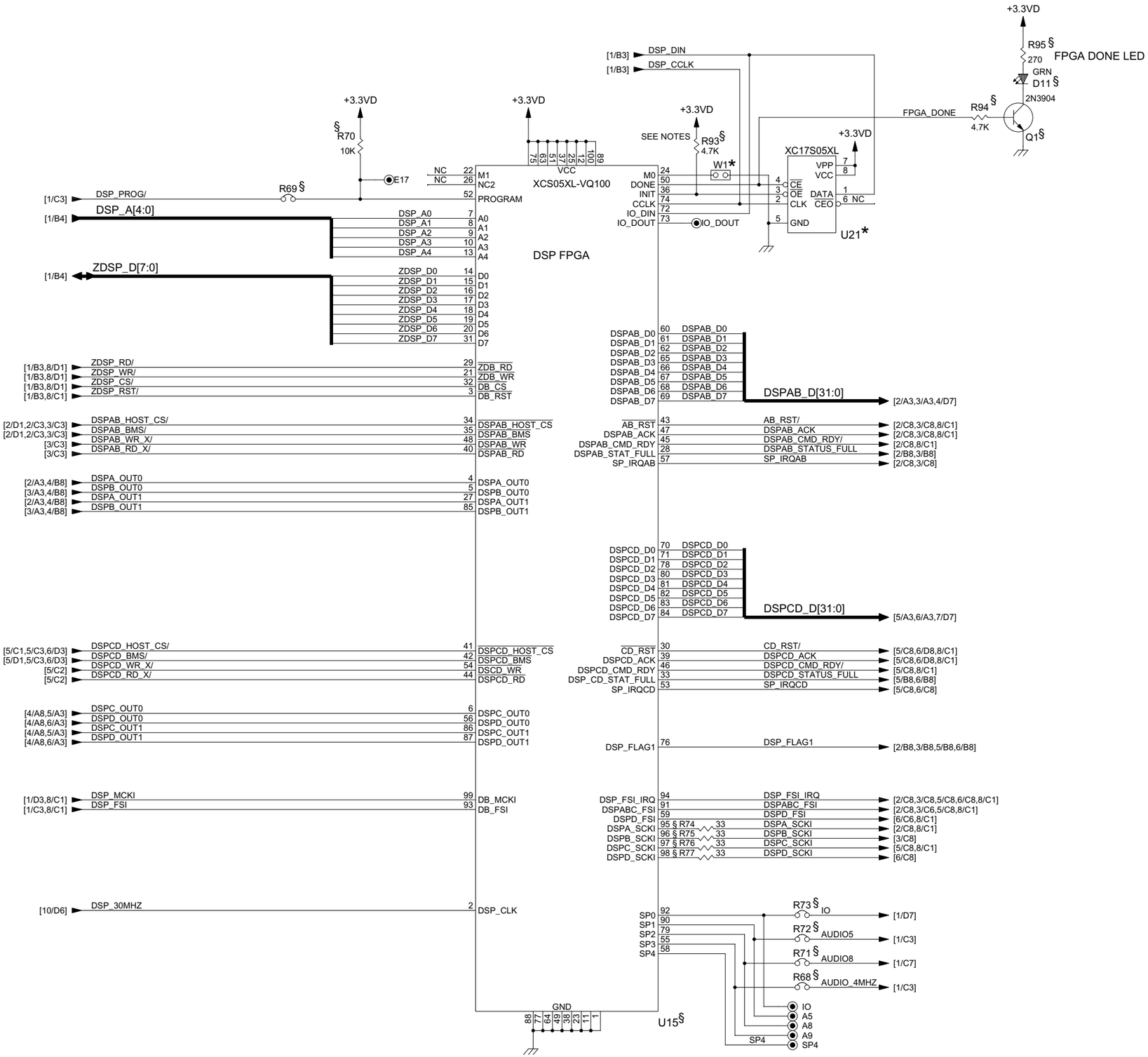
TITLE
SCHEM,MIC/DSP BD,MC8
DSPCD EXT MEM

SIZE	CODE	NUMBER	REV
B		060-15389	1

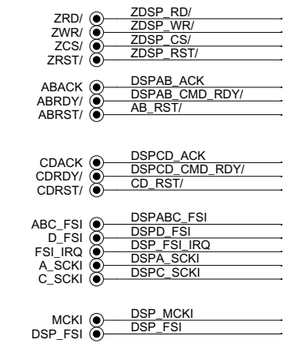
FILE NAME 15389-2.7 SHEET 7 OF 10

12-15-2004_8:52

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REVISED SIGNAL NAMES PER DCR 020926-00	CW 9/27/02	RWH 10/15/02
		KAB 10/11/02	KAB 10/15/02
2	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04



TEST POINTS



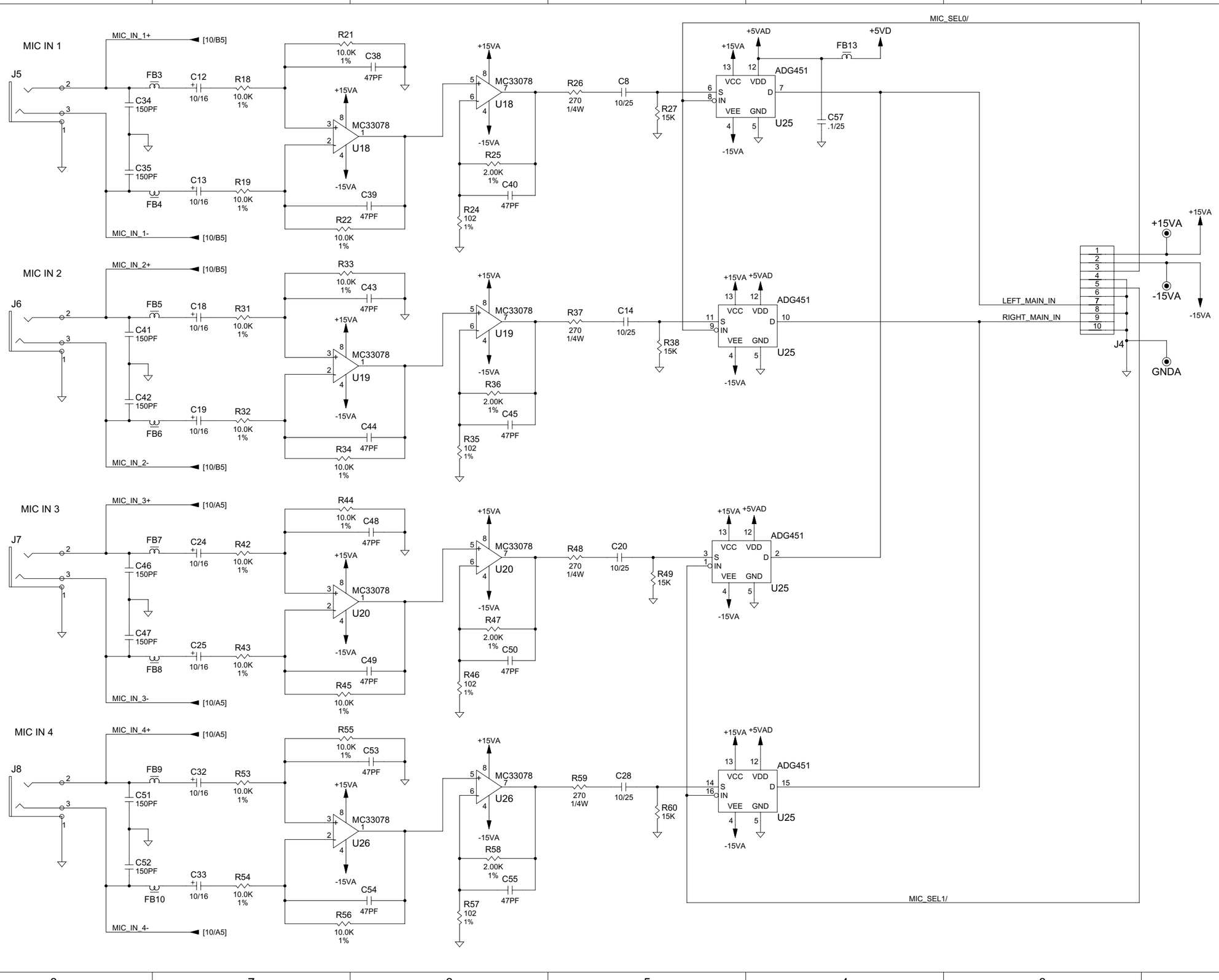
NOTES

1 M1,M0 HAVE WEAK PULLUPS
M1,M0 = 1,1 SLAVE SERIAL MODE
M1,M0 = 1,0 MASTER SERIAL MODE

2 JUMPER W1 TO GND TO USE CONFIGURATION ROM.

CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS		DATE	TITLE: SCHEM,MIC/DSP BD,MC8 FPGA
DRAWN	RWH	5/20/02	
CHECKED	KB	5/29/02	SIZE: B; CODE: ; NUMBER: 060-15389; REV: 2
Q.C.	CW	6/3/02	
ISSUED	KB	6/3/02	FILE NAME: 15389-2.8; SHEET 8 OF 10

12-15-2004_8:52



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

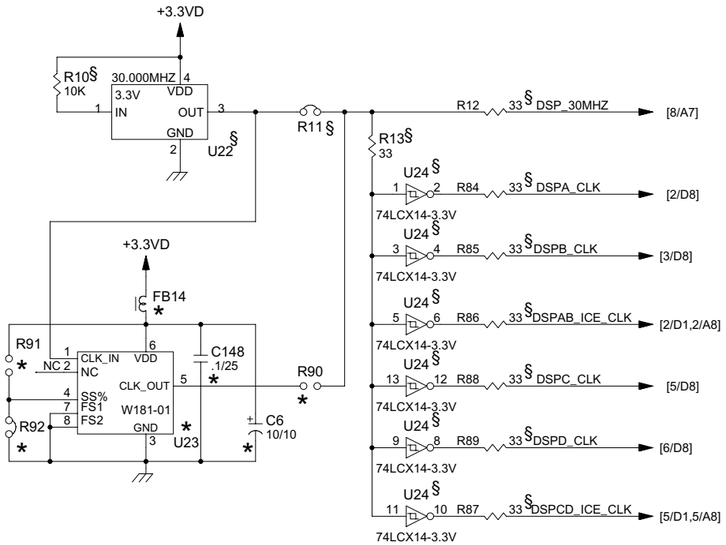
APPROVALS		DATE
DRAWN	RWH	5/20/02
CHECKED	KB	5/29/02
Q.C.	CW	6/3/02
ISSUED	KB	6/3/02

TITLE: SCHEM,MIC/DSP BD,MC8 MICROPHONE INPUTS

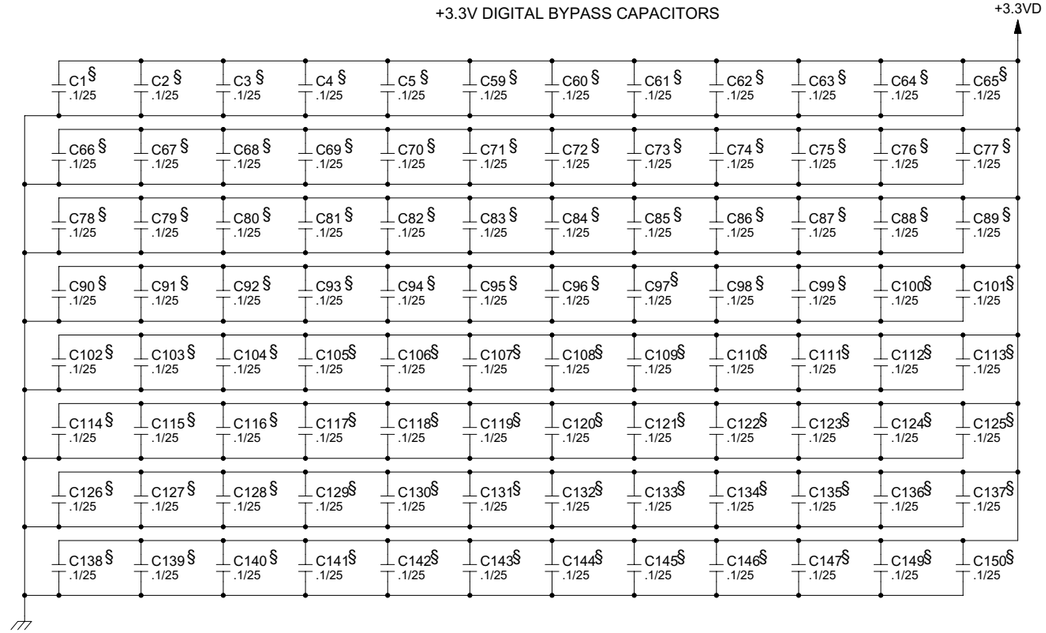
SIZE	CODE	NUMBER	REV
B		060-15389	0

FILE NAME: 15389-2.9 SHEET 9 OF 10

12-7-2004_10:16

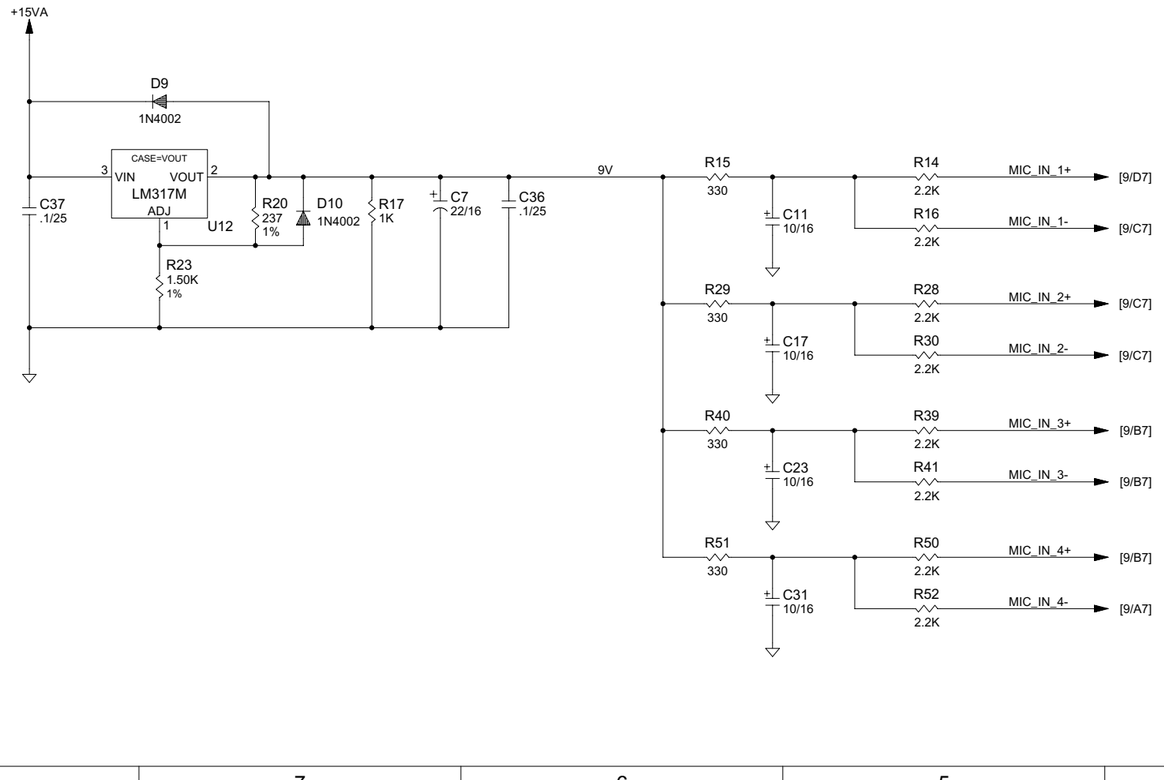


+3.3V DIGITAL BYPASS CAPACITORS

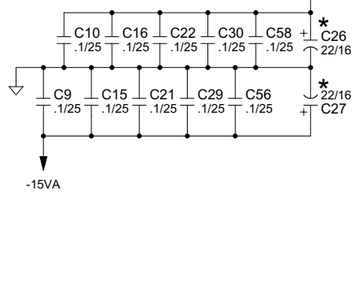


REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	SHOW DEPOPULATION FOR MIC BD. PER ECO 041201-00.	RWH 12/7/04	CW 12/14/04
		AF 12/9/04	MSJ 12/9/04

MICROPHONE BIAS VOLTAGE SUPPLY



BYPASS CAPACITORS



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

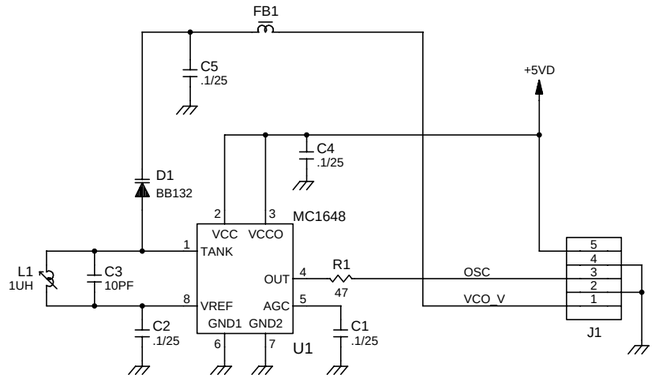
APPROVALS		DATE
DRAWN	RWH	5/20/02
CHECKED	KB	5/29/02
Q.C.	CW	6/3/02
ISSUED	KB	6/3/02

TITLE: SCHEM,MIC/DSP BD,MC8
BYPASS CAPACITORS & DSP CLOCKS

SIZE	CODE	NUMBER	REV
B		060-15389	1

FILE NAME: 15389-2.10 SHEET 10 OF 10

12-15-2004 8:52



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND

5 LAST REFERENCE DESIGNATORS USED: C5, D1, FB1, J1, L1, R1, U1.

REFERENCE COPY

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	3/3/03
CHECKED	ECM	3/5/03
Q.C.	CW	3/7/03
ISSUED	KAB	3/11/03

TITLE: SCHEM, VCO BD, MCLK

SIZE	CODE	NUMBER	REV
B		060-16139	0

FILE NAME: 16139-0.1 SHEET 1 OF 1

3-18-2003_9:15

Harman Specialty Group 3 Oak Park, Bedford, MA, 01730-1413 USA
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Part No. 070-17536 | Rev 0